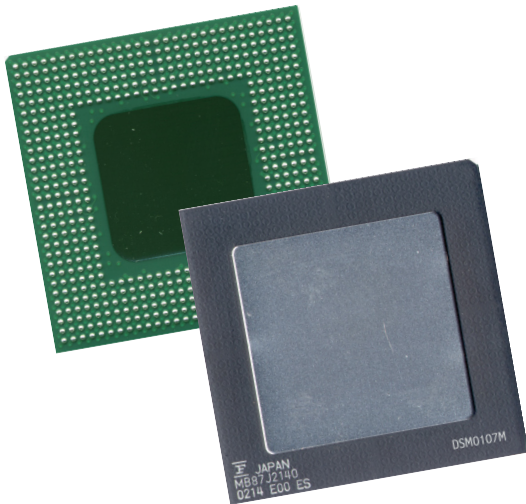


## Digital Signal Memory (DSM) System-On-A-Chip

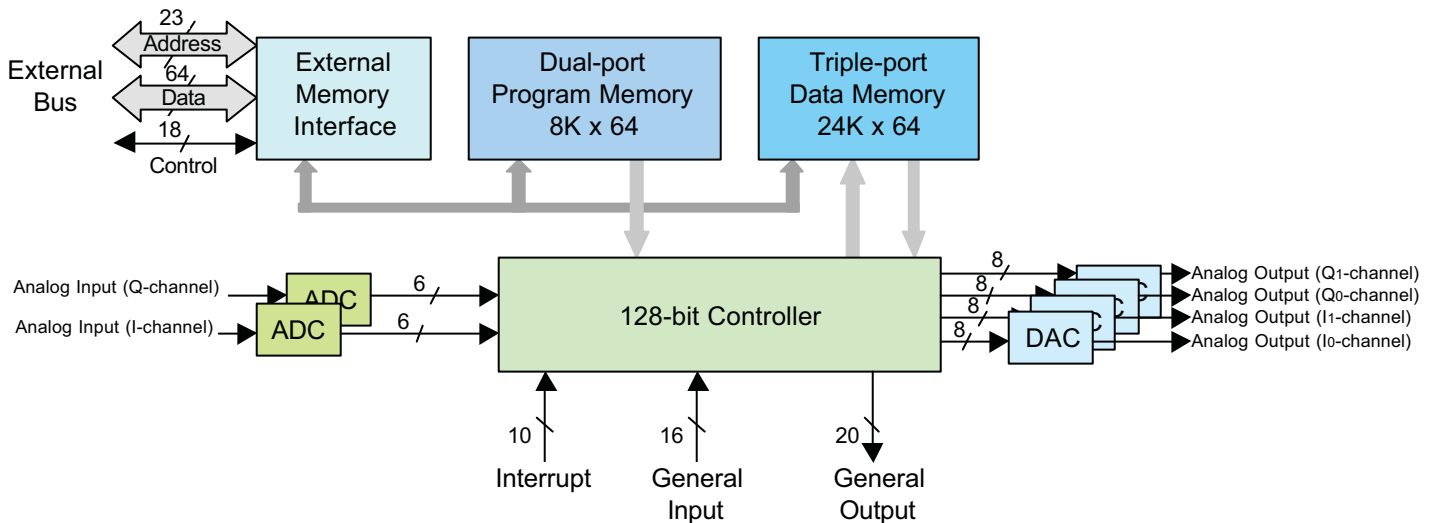


DSM is high performance accumulation and signal processing System-On-A-Chip with integrated ADCs and DACs that is used in digital signal-processing systems. 2 MB on-chip SRAM allows to receive and to store high frequency analog signals of duration up to 655 $\mu$ s. A number of programmable counters and multiple internal and external interrupts provide the output of pulse and periodical high frequency analog signals stored in on-chip SRAM with required delays and durations in real time. Internal high speed arithmetic units provide the programmable amplification of input signals, their summation with output signals, and programmable Doppler shift for output signal. The 64-bit external bus provides fast instruction and data transfers between DSM and external memory or host DSP both in DMA and in random access mode.

### Features:

- Synchronization from external source with frequency  $F_s$  from 5 MHz up to 600 MHz.
- Two 6-bit ADCs convert quadrature components I and Q of input signal with input sample rate  $F_s$ ,  $F_s/2$  and  $F_s/4$  up to 600 MSPS.
- Four 8-bit DACs form even and odd samples of quadrature components I and Q of output signal with output sample rate  $F_s/2$ ,  $F_s/4$  and  $F_s/8$  up to 300 each.
- Digital processing of quadrature components of input and output signals:
  - Input signal detection.
  - Maximum amplitude of input signal calculation.
  - Time fixation of the coincidence of I and Q quadrature components of input signal.
  - Digital amplification of input signals.
  - Addition of input signal with output or reference signal.
  - Programmable delay for pulse and programmable frequency for periodical output signals with step of 13.33 ns (minimum propagation delay from analog input to analog output is 35 ns).
  - Programmable Doppler shift for output signal at range from -250 KHz up to 250 KHz with step of 8,94 Hz.
  - Mixing of two output signals (the mixing frequency is from 18,75 MHz up to 75 MHz).
- Programmable digital interface - 16 inputs and 20 outputs.
  - Maximum operating frequency for digital interface - 150 MHz.
- 64 Kbytes on-chip dual-port instruction memory.
- 192 Kbytes on-chip triple-port data memory.

### DSM Functional Diagram



- Programmable external memory interface with 64- or 32-bit data bus.
  - Three types of external memory support: SRAM, SSRAM and SDRAM.
  - Maximum data transfer rate for SRAM - 600 Mbytes/s.
  - Maximum data transfer rate for SSRAM and SDRAM - 800 Mbytes/s.
  - Address space for external memory - 64 Mbytes.
  - Shared memory mode for the controller and external processor.
  - Random access mode of external processor to internal memory of DSM.
- 10 external and 140 internal interrupts.
- 24-bit real time counter.
- 8 on-chip programmable channels, each of which contains DMA channel, 18-bit delay counter, 12-bit event counter and also the hardware to generate interrupts when some internal or external event has occurred.
- Cycle time for program controller - 6.666 ns (150 MHz).
- Main data format - 64-bit words of packed one byte data of two's complement representation.
- Bit length of instructions - 128. Each instruction is executed per two cycles.
- 2,300,000 equivalent gates.
- CMOS 0.25  $\mu\text{m}$  technology.
- Power supply - 3.3 V and 2.5 V.
- Power consumption - not more than 4.2 W.
- Operating temperature range - from  $-40^{\circ}\text{C}$  up to  $+85^{\circ}\text{C}$ .
- 576 Ball Grid Array (BGA).