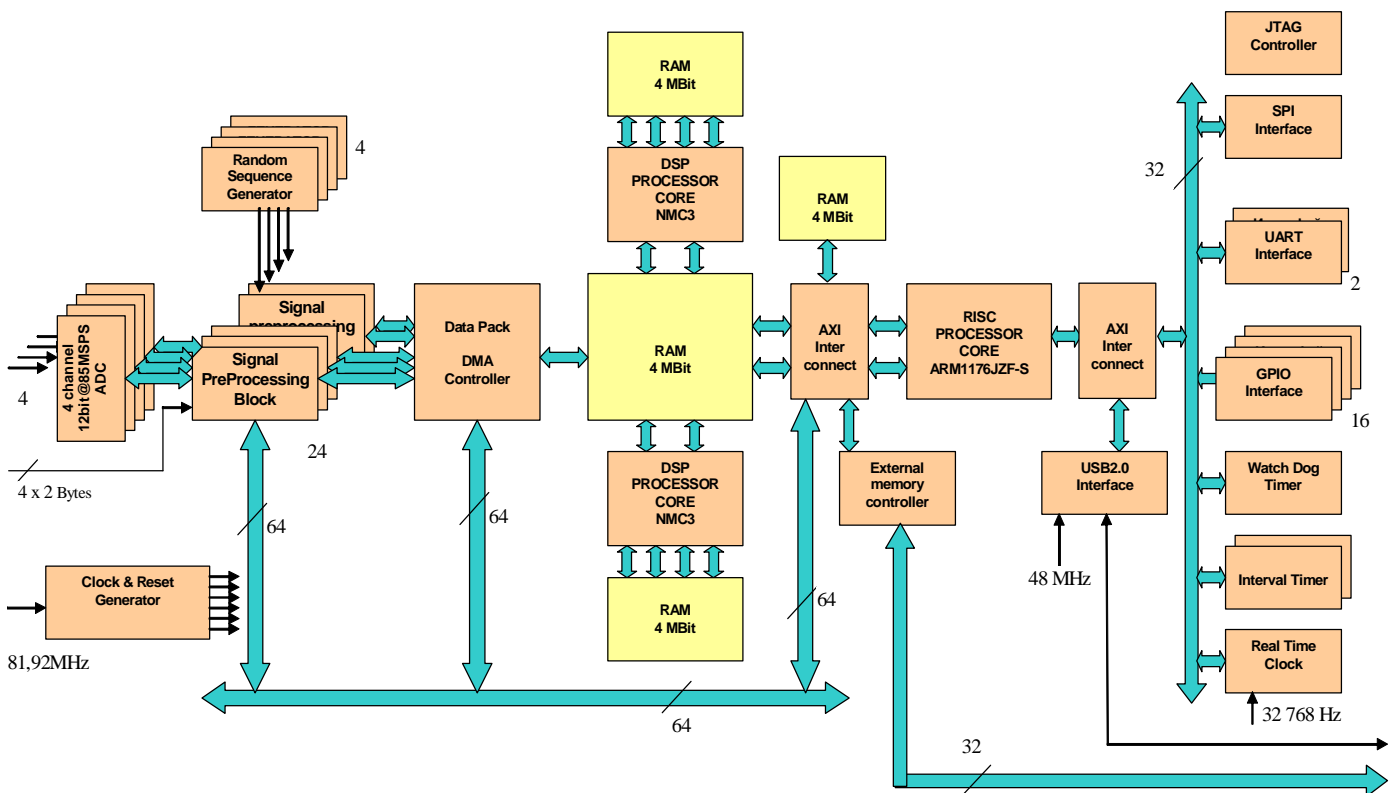


NeuroMatrix® 1879XK1 Programmable Baseband Processor SoC

The NeuroMatrix® 1879XK1 baseband processor (BBP), a mixed signal System-on-a-Chip (SoC), is unified programmable digital receiver, designed for analog to digital signal conversion, frequency mixture, digital filtering, preliminary and final digital signal processing for a broad range of Software Defined Radio (SDR) devices. The BBP SoC comprises of 4-channel ADC, 2 NMC3 DSP cores and one ARM1176 RISC processor core. NeuroMatrix® Core 3 (NMC3) is a high performance DSP core with VLIW/SIMD decoupled architectures. The core includes a 32/64-bit RISC processor and a patented 1-64-bit VECTOR co-processor to support vector operations with elements of variable bit length. The NMC3 is developed for math-intensive real-time vector/matrix operations under variable 2-64-bits width data flow. Two on-chip NMC3 cores ensure effective implementation of FFT, WHT, convolution, correlation and other basic DSP algorithms. Powerful 32-bit ARM11 RISC core with vector FPU performs a general purpose computations and control functions.



BBP SoC Block Diagram

Targeting Applications

- § multi band and multi system GLONASS / GPS / GALILEO / COMPASS receivers with Safety-of-Life (SoL) features
- § telecommunication
- § digital radio

- § radars
- § GSM, CDMA etc.
- § wide range of digital signal processing for SDR, general purpose computations and control functions.

Key technical characteristics

- § Four channel 12bit@85MSPS ADC
- § Signal PreProcessing hardware block
- § Two 64-bit NeuroMatrix® NMC3 DSP cores
- § 32-bit ARM1176-JZF RISC-core with vector FPU
- § 16Mb RAM
- § DDR1 memory controller
- § UART, SPI, USB2.0, GPIO interfaces
- § JTAG (IEEE Std. 1149.1) controller

Signal PreProcessing hardware block functions

- § 40MHz baseband signal bandwidth
- § Internal digital frequency heterodyne oscillator
- § Digital frequency heterodyne with quadrature I/Q components generation
- § First stage Signal samples accumulation
- § Noise suppression with FIR filter
- § Second stage samples accumulation with programmable step
- § Accumulated signal normalization
- § Sort, pack and write signal frames into the memory
- § Accurate time frames forming in range of 25 micro seconds to 1.63 s with 25 micro seconds step
- § Accurate 1 sec pulse forming
- § Time forming accuracy is 3ns
- § Pseudorandom sequence generation.

BBP SoC features

§ technology	CMOS 90nm
§ input analog signal bandwidth	up to 40 MHz
§ 12-bit resolution 85M samples per second ADC	
§ Number of ADC	4
§ Number of Signal PreProcessing hardware channels	24
§ Digital heterodyne frequency range	0 – 40.96 MHz
§ Digital heterodyne frequency step	0.6 Hz
§ FIR filter – coefficients	8/16 bits
§ FIR filter – number of taps	64 – 256
§ FIR filter – sample rate	20.48 MSPS
§ FIR filter – total number	up to 12

§ Accumulation range	1 - 2048
§ Squarer units number	12
§ DSP processor core	NMC3, 2 cores
§ RISC processor core	ARM1176JZF-S
§ On-chip RAM	16 Mb
§ Serial interfaces	2 UART, SPI, USB2.0, 16 GPIO
§ DDR1 Memory interface 32-bit up to 166 MHz	up to 10,6 Gb/s
§ Core power supply voltage	1,2±0,1V
§ External buffers power supply voltage	3.3 ±0.3V, 2.5 ±0,2 V
§ Analog macro power supply voltage	1,2V, 3,3V
§ Ambient temperature range	-40 ... +70 °C
§ External clock signal	up to 82 MHz
§ External crystal generators	48 MHz, 32 768 Hz
§ Power consumption (depends on operation mode)	0.5 –2.0 W
§ Power consumption in standby mode	< 0.15 W
§ Die size	72 mm ²
§ Package type	BGA484
§ Package dimensions	27mm x 27mm x 2.36mm
§ Pin number	484

The unique technical features of BBP SoC ensure its effective implementation in ready-to-use professional multi system jam-resistant navigation devices for intelligent transport systems applications, avionics and marine navigation, including Safety-of-Life services and applications with high level guarantee of signal receiving. Furthermore BBP chip is fitted with special alert system for the case of diminishing signal precision based on up-to-date concepts of GNSS development.

BBP chip architecture provides signals receiving and processing with all existing GNSS (up to 4 signal types simultaneously), moreover it will ensure adoption for receiving and processing signals of forthcoming GNSS without any hardware modifications. This functionality assures high level of signal noise-immunity and precision so as the navigation device can use different frequency bands and signal structures.

Besides mentioned navigation tasks BBP SoC also can be effectively used in different applications for digital signal processing, digital radio broadcasting, radar, cellular signal processing etc.

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