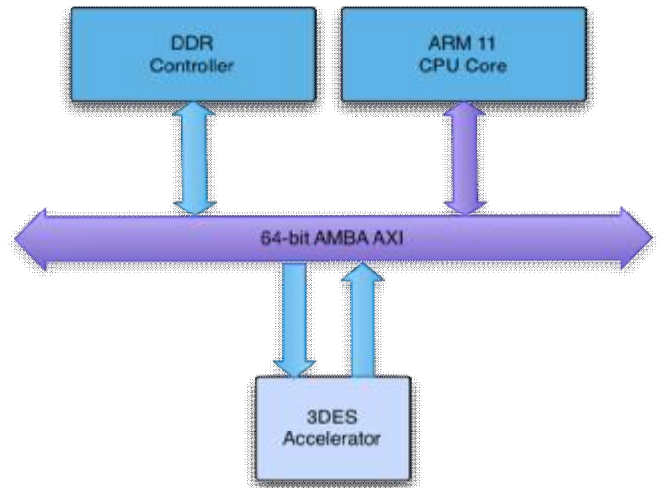


## IP core Hardware 3DES Accelerator

### Key Features

- Streaming encryption/decryption of large data blocks in DMA master mode
- Single-word operation mode
- High performance:
  - 12 bus cycles per block for 3DES
  - 4 bus cycles per block for DES
- ECB and CBC modes support
- ATSC descrambling extensions
- FIPS 46-3 compliant
- Linux CryptoAPI drivers



### Technical characteristics

- Designed for low latency and high throughput applications in embedded systems
- Specially optimized for hardware acceleration of Linux CryptoAPI subsystem
- DES/3DES encryption and decryption
- ECB & CBC modes
- All possible 3DES options are supported (EEE, EED, EDE, EDD, DEE, DED, DDE, DDD)
- Complete implementation of FIPS 46-3
- ATSC descrambling is supported for DTV applications (support for short-blocks in 3DES-CBC mode)

### Performance

- 4 bus cycles for DES
- 12 bus cycles for 3DES
- Asynchronous bulk operations in DMA mode for high performance on large data sets
- Synchronous single-word operations for low-latency encryption operations, can be executed during bulk asynchronous transaction

### Interfaces

- 32-bit AMBA APB Interface
- 64-bit AMBA AXI Master
- Linux CryptoAPI drivers are available

### List of Deliverables

- Verilog source code
- Verilog test bench and Verification environment
- Software driver for Linux OS
- Example synthesis scripts
- Documentation

### Size

- 50K gates

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