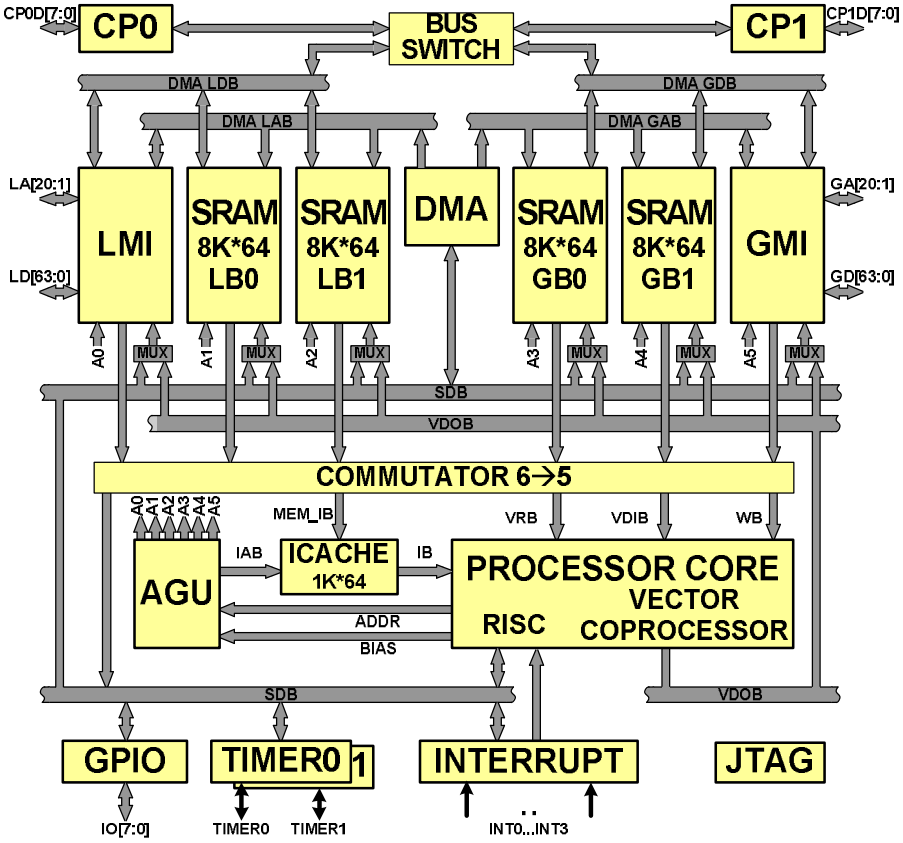
NeuroMatrix® NM6405 DSP

NM6405 is a high performance DSP oriented RISC processor designed for real time data flow processing. The architecture is based on the advanced VLIW/SIMD NMC3 core, and consists of a 32/64-bit RISC processor and a 64-bit VECTOR co-processor. The co-processor supports vector/matrix operations with elements of variable bit length (US Pat. 6539368 B1).

Features

- 32/64-bit RISC processor core;
- 64-bit vector coprocessor (VECTOR COPROCESSOR);
- Four dual port internal SRAM banks (8Kx64 bit each);
- 1Kx64bit of instruction cache memory (ICACHE);
- Address generator unit (AGU);
- Two 64-bit external memory interfaces (LMI и GMI), that operate at speed up to 130 MHz;
- Two Byte communication ports with throughput each up to 150 MB per second;
- Eight general purpose IO ports (GPIO);
- JTAG port for debug and test purposes;
- Two independent DMA controllers;
- Internal/External interrupts controller (INTERRUPT);
- Two universal 32-bit timers (TIMER0 и TIMER1).



NM6405 DSP Functional Diagram

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Main characteristics

- CMOS technology – 0.25u;
- package – 576 BGA

- Clock frequency – 150 MHz;
- Power supply – 2,5 V (core) 3,3 B (I/O buffers);
- Power consumption – less than 3,8 W;
- Ambient temperature: -55°C … +85°C.

RISC processor

- Data width – 32 bit;
- Instruction width – 32 и 64 bit;
- Address space – 4Gx32 bit;
- 3 scalar instruction per clock cycle (ALU operation, address modification input/output operation);
- Performance – 150 MIPS (450 MOPS).

Vector coprocessor

- Programmable data length from 2 to 64 bits (64bit length data words packed);
- Basic operation is integer data matrix multiplication by integer data matrix;
- Concurrent execution of 2 saturation operation with input data flow;
- Performance (MAC – Multiplication and Accumulation per clock cycle) –
  2 MAC for 32-bit data;
  4 MAC for 16- bit data;
  24 MAC for 8- bit data;
  80 MAC for 4-p bit data;
  224 MAC for 2- bit data.

Applications

- hydro- and radiolocation;
- IR and video processing;
- Artificial Neural net emulation;
- Navigation;
- CDMA и TDMA base stations;
- Vector and matrix computations.

The NM6405 processor is oriented for massive dataflow processing with short bit length signal samples.
The software design kit NM-SDK Version 3.0 includes an optimizing C++ compiler (ISO/IEC 14882:1998 standard), assembler, disassembler, linker, debugger and real-time DSP and NeuroMatrix® Processing Library (NMPL). The compiler adheres to the C++ standard, including templates, and uses the enhanced optimizing algorithms that allow increasing program execution speed and decreasing code size. The assembly language has an intuitive syntax and is close to high-level languages so it can simplify the development and understanding of source code for math-intensive real-time algorithms.
Single DSP Evaluation Board with PCI interface can be used for software design.

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