

## NeuroMatrix<sup>®</sup> Core (NMC)

**NMC** is a synthesizable Verilog RTL model of a high performance DSP core with VLIW/SIMD architecture. The core includes two main units: 32-bit RISC processor and 64-bit VECTOR coprocessor to support vector operations with elements of variable bit length (Pat. 2131145 RU).

### Features:

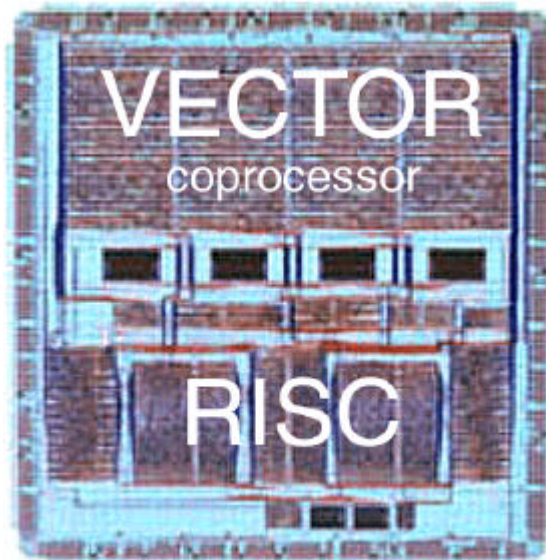
- Silicon proven (NM6403 DSP)
- Scalable DSP performance
- Original instruction set
- Small number of eq. gates (~80.000)
- Clock frequency - 123 MHz (8ns instruction cycle time) at 0,25 um CMOS technology
- Strong Software Development Kit
- PCI Evaluation Board

#### *RISC Processor*

- 5-stage pipelined 32-bit RISC
- Processor instructions are 32 and 64-bit wide (usually two operations are executed by each instruction)
- Two address generation units, address space - 16 GB
- Two wide 64-bit data buses
- Data format: 32-bit digit integers
- Registers:
  - ⇒ 8 of 32-bit general purpose registers
  - ⇒ 8 of 32-bit address registers
  - ⇒ special control and state registers

#### *VECTOR co-processor*

- 1-64 bit word length of vector operands and the products
- Data format: integer data packed into 64-bit blocks in the form of variable length words from 1 to 64-bits each
- Hardware support of vector-matrix or matrix-matrix multiplication
- On-chip saturation functions
- On-chip three 32\*64-bit RAM blocks



NM6403 DSP Layout

### Applications:

- Core for traditional DSPs:
  - ⇒ image processing
  - ⇒ signal processing
  - ⇒ neural net emulation
  - ⇒ acceleration of vector and matrix calculations
- Telecommunication chips
- 3G Wireless Digital Baseband Processors
- Crypto-processors
- Embedded processors
- Basic block for building System-On-A-Chip

### Performance:

- Scalar operations:
  - 1\*F MIPS, where F is a clock rate in MHz
  - 3\*F MOPS for 32-bit data, where F is a clock rate in MHz
- Vector operations:
  - from 1\*F up to 288\*F MMAC (million multiplication and accumulation per second), where F is a clock rate in MHz