

**THE LIST OF RESOURCES  
SUPPORTING DIGITAL-  
SIGNAL PROCESSING  
CONTINUES TO EXPAND.  
CHECK OUT THE  
LATEST ADDITIONS.**

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2004

# DSP DIRECTORY

WELCOME TO the 2004 edition of the *EDN* DSP directory. Despite some companies dropping out of the DSP market, whether due to acquisition or a redirection of marketing focus, the DSP directory continues to grow. In response to this continued growth, this year's print version of the directory is an incremental update of last year's report. This fact means that the 2004 version includes only new or changed information, and you need the 2003 version, which you can find with the 2004 version on the *EDN* Web site ([www.edn.com](http://www.edn.com)), to see all of the relevant material. Be sure to examine the 2004 directory index to see what information is new and what old information is obsolete. Companies that the 2004 index does not list are obsolete in the 2003 version. Next year's directory will combine these two versions and any new material that surfaces between now and then.

As for the DSP market, according to market-research company Forward Concepts ([www.fwdconcepts.com](http://www.fwdconcepts.com)), the market for general-purpose programmable DSPs reached \$6 billion in sales in 2003, which represents a 24% growth from the previous year. Communication, especially cellular, and consumer applications are the large drivers for the DSP market. Forward Concepts forecasts a 25% growth for the DSP market for 2004.

As signal-processing designs become more complex, device and IP (intellectual-property) vendors are developing and packaging bundled resources, platforms, or reference designs to demonstrate how customers can use their offerings for applications. These reference designs are becoming important strategic-design-win tools and may go beyond design samples and application notes, even to the point in some cases of turnkey implementations. Finding a vendor's reference designs is currently neither straightforward nor consistent



within a vendor's product material. You should this year begin seeing changes in how vendors will disseminate their reference designs to the engineering community.

Another emerging change in how companies are marketing DSPs reflects what many design engineers have known all along: that they can efficiently implement signal processing using one or more types of signal-processing engines, such as software-programmable DSPs, fixed-function devices, reconfigurable devices, and host microprocessors. Standard processor devices with dual DSP and RISC cores and the development tools that support these devices are becoming more common.

An example of this emerging marketing shift is the public position that Texas Instruments and Xilinx are taking; their products are complementary rather than competitive. The standard DSP devices represent an implementation for the lowest cost and the lowest power consumption with the right amount of performance for required and commodity functions. Configurable devices, such as FPGAs, provide a method to implement new innovations that differentiate a design. As a func-

tion that a designer may originally implement on an FPGA matures and finds its way into high-volume designs, a designer may eventually integrate it into an ASSP (application-specific standard part) that may preclude cost-effectively using it on the FPGA again. As ASSPs usurp and integrate these common functions, such as FFT butterflies and Viterbi decoders, the function space for FPGAs will need to move forward to include new innovative functions.

In response to this acknowledgment of the complementary nature of the ways to implement signal processing, the DSP directory is incorporating devices and IP offerings beyond just the software-programmable devices and cores, as in previous years. This goal will probably present some categorizing challenges, especially with narrowly defined and specialized ASSPs and IP blocks, but it is a challenge *EDN* will address with each new addition to the directory. If you have ideas for how to incorporate the types of signal-processing options, including reference designs and platforms, please share them with us by e-mailing your ideas to [dspdirectory@edn.com](mailto:dspdirectory@edn.com).

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## AGERE SYSTEMS

Agere's 16-bit DSP16411, a high-performance device targeting low system cost for wired and wireless infrastructure applications, is the latest addition to the DSP16000 device family. The DSP1641X architecture and instruction set include optimizations that target communications-infrastructure applications. The DSP16411 increases the operating frequency by 45% to 285 MHz versus 195 MHz and increases the on-chip memory by 66% to 640 kbytes from 384 kbytes in the same device footprint as the DSP16410. The DSP16411 features twin DSP16000 dual-MAC (multiply-accumulate) DSP cores and enhanced-DMA capabilities. Each DSP core has access to a 320-kbyte block of memory (640 kbytes total) and shares a 4-kbyte block of memory for interprocessor communications. The DSP16411 is board-design-, pinout-, and code-compatible with the DSP16410C.

Agere's LUXWorks development tools now support the Linux operating system, an upgrade to the latest version of Tcl/Tk (Tool Command Language/Tool Kit), and a new Windows2000/XP TargetView driver. LUXWorks runs natively on Windows 95, 98, ME, 2000, and XP in both simulation and hardware modes, supports native simulation and networked hardware mode on the many Solaris and Linux platforms, and supports tools from Cadence, CoWare, Mentor Graphics, and Synopsys on Solaris. Agere supports an online knowledge base that includes application notes, reference designs, and software. Agere is one of the co-founders of StarCore and continues to offer the synthesizable StarCore DSP technology for integration into custom designs.

**ALTERA** Altera manufactures Stratix II FPGA devices on 300-mm wafers using TSMC's 90-nm all copper, low-K dielectric-process technologies. The devices incorporate as many as 180,000 equivalent logic elements and 9 Mbits of RAM, and they support migration to HardCopy structured ASICs. The company manufactures Cyclone FPGA devices on an all-copper, 1.5V SRAM process that delivers as many as 20,060 logic elements and 288 kbits of RAM. The Cyclone family offers multiple full-featured PLLs to manage board-level clock networks and dedicated I/O interfaces to connect with external memory devices. The Cyclone device family supports Altera's Nios embedded processor and IP (intellectual-property) portfolio.

SOPC (system-on-programmable-chip) Builder enables designers to build power platforms by composing bus-based systems from common system components. System designers can define a system—from hardware to software—within a single tool. The SOPC Builder library components range from simple fixed-logic blocks to complex, parameterized, and dynamically generated subsystems. These library components include processors; IP; peripherals, such as memory interfaces, communications peripherals, buses and interfaces, and DSP IP; and software, such as header files, generic C drivers, and operating-system kernels.

Altera's DSP Builder tool uses the Quartus II development software to interface with The Mathworks' system-level DSP

tool, Simulink, and allows designers to port algorithms they develop with The Mathworks' ([www.mathworks.com](http://www.mathworks.com)) Matlab and Simulink software to HDL (hardware-description-language) files. DSP Builder automatically generates a RTL (register-transfer-level) design and RTL testbench from Simulink. These files are preverified RTL-output files for use in Quartus II design software for timing and simulation comparisons. The design flow also enables floating-point-to-fixed-point analysis.

Quartus II 4.0 software supports the Stratix II FPGA family of devices and enables designers to perform I/O assignment and validation before design modules are available, so pc-board layout can begin earlier in the process. The software supports EDA tools available for FPGA design and includes command-line and tool-command-language interfaces similar to those in many third-party EDA tools.

The SignalTap II embedded logic analyzer enables designers to capture the state of internal nodes or I/O pins while the device is running in system and at system speeds. It requires neither external probes nor changes to user-design files to capture a design's state of internal nodes or I/O pins. The SignalTap II analyzer supports multiple devices in a single JTAG chain, as many as 1024 channels with as many as 128,000 samples per channel, and acquisition clocks operating as fast as 200 MHz. SignalTap II supports development for Stratix, Stratix II, and Cyclone FPGAs.

Altera's MegaCore FIR compiler implements signal filtering to remove unwanted noise, provide spectral shaping, or perform signal detection or analysis for Stratix II, Stratix, and Cyclone devices. The FIR compiler finds the coefficients to design a FIR filter with a set of characteristics, and it generates cycle-accurate FIR-filter models in Verilog HDL, VHDL, model format for the Matlab environment, and device-specific code for the Quartus II software.

The FFT MegaCore function is a parameterizable FFT processor that includes a quad-output, radix-4 FFT engine that integrates an FFT, data RAM, and twiddle ROM. It includes an Atlantic interface and IP-functional simulation models for use in Altera-supported VHDL and Verilog HDL simulators.

## ANALOG DEVICES

High-end Analog Devices Blackfin processors can now operate at 750 MHz because of architecture updates and an increase in the power-supply voltage from 1.2 to 1.4V. The ADSP-BF561 retains full code compatibility with the ADSP-BF533 and includes the dynamic-power-management capabilities of the Blackfin architecture. The ADSP-BF561 integrates two Blackfin processor cores, each of which can operate as fast as 750 MHz. The device integrates 328 kbytes of on-chip memory and includes 16 kbytes each of instruction cache and SRAM, 32 kbytes each of data cache and SRAM, and 4 kbytes of scratchpad SRAM. Additional on-chip memory peripherals include 128 kbytes of L2 SRAM, a four-channel DMA controller, and an external memory controller supporting any SDRAM, SRAM, flash, and ROM options. The ADSP-BF561 includes dual parallel-peripheral-interface units that support



ITU-R 656 video-data formats; two dual-channel, full-duplex synchronous serial ports supporting eight stereo I<sup>2</sup>S channels; a UART with IrDA support; and an on-chip PLL. Packaging options include miniBGA and a sparse PBGA. Green Hills' ([www.ghs.com](http://www.ghs.com)) Multi IDE tool suite now supports development with the Blackfin processor.

The third-generation SHARC processors, such as the ADSP-21266 and ADSP-21267, target consumer, automotive, and professional-audio applications. The new pin-compatible SHARC devices increase the operating frequency to 300 MHz and increase the on-chip memory to up to 4 Mbits of ROM and 3 Mbits of RAM. The integrated S/PDIF receiver/transmitter eliminates the need for an external PLL or clock. The processors integrate a sample rate converter for multichannel audio, offering as much as 140 dB SNR and dynamic range, as well as 192-kHz sample rates. The Digital Transmission Content Protection Accelerator for encryption/decryption of digital-audio data over networks provides as many as 20 channels of I<sup>2</sup>S support. The new SHARC processors are certified for running Microsoft WMA 9 Pro (Windows Media Audio 9 Professional) and Dolby Pro Logic Ix. The processors also support PCM 96 kHz, Dolby Digital, Dolby Digital EX, DTS Discrete 6.1, DTS-ES Matrix 6.1, DTS 96/24 5.1, DTS Neo 6, MPEG-2, and MPEG-2 AAC (Advanced Audio Coding).

The ADSP-TS20x is the latest addition to the TigerSHARC processor family, and it boasts 24 Mbits of embedded DRAM that is organized into six non-hierarchical, 4-Mbit memory blocks, each effectively operating at core speed. The ADSP-TS20x includes four 128-bit-wide internal buses to support simultaneous access of four of the six memory banks. A new LVDS (low-voltage-differential-signal) link port enables a proportional increase in I/O bandwidth to 5 Gbytes/sec of throughput with the increase in multiply-accumulates and floating-point operations per second. Like other TigerSHARC processors, ADSP-TS20x processors include four parallel link ports that operate in the background and multitask with the core to enable data to move into and out of the processor, such as for multiprocessor applications.

**ARM** ARM acquired the OptimoDE Data Engine technology when it acquired part of Adelante Technologies last year. The OptimoDE technology is licensable intellectual

## ATMEL

Atmel's mAgic DSP core is a floating-point, complex-domain, 40-bit precision VLIW (very-long-instruction word) DSP core that targets complex-domain, floating-point, embedded-system applications, including professional-quality audio, speech processing, radar-based collision avoidance, acoustic diagnosis, and software-based ultrasound scanners. The mAgic DSP can perform 15 operations per cycle, 10 of which are floating-point, and it supports pipelined, single-cycle execution of complex arithmetic. The mAgic core has 10 floating- and fixed-point operators, including four multipliers, three adders, and three subtractors, which are arranged in two identical parallel blocks. The data memory comprises 512 40-bit registers, arranged in two banks of 256 registers each. A dedicated datapath between the two register banks allows you to use them as a single bank of 256 "complex registers" for the simultaneous execution of both real and imaginary arithmetic. The mAgic VLIW code compression achieves code density of four program-memory bits per floating-point arithmetic operation and an average effective code density of 50 bits per stored VLIW-instruction cycle without a loss of performance.

Atmel's Diopsis dual-processor catalog-product DSP integrates the mAgic core with an ARM7 microcontroller core, memories, and peripherals. The data-memory architecture reduces the number of memory-fetch cycles by supporting two read and two writes per cycle to the internal, 80-kbyte dual-port data memory that comprises two sets of three 2048×40-bit pages, plus two 2048×40-bit data buffers to the external-memory interface. An 8096×128-bit, single-port program memory stores approximately 24,000 instruction cycles of compressed mAgic code. Diopsis supports single-cycle execution of FFT butterflies, complex multiply accumulate, and real-domain dual MACs (multiply/accumulates). The Diopsis can perform a 1024-point FFT in 5962 cycles.

The complex-domain arithmetic and floating-point core preclude the need to translate floating-point-based algorithms to fixed-point implementations. Atmel's MADE (multicore-application-development environment) includes C compilers for both the ARM and the mAgic DSP; a high-level mAgic DSP macroassembler/optimizer; the eCos RTOS; a unified debugging environment; and a library of 75 C-callable DSP functions, including FFTs, IIRs, FIR on single-sample sequence or input-data-frame stream, vectorial square roots, vectorial magnitudes, and vectorial arithmetic operations. You can program both Diopsis cores entirely from the ARM programming interface, using calls from the mAgic DSP library to execute DSP functions. Alternatively, you can separately program the RISC and the DSP. The 5000-instruction/sec cycle-accurate and 2 million-instruction/sec instruction-accurate simulators provide visibility into the memory and registers of both processors for simultaneous debugging of the entire Diopsis system.

property with an associated tool environment to be deployed alongside an ARM microprocessor core. The VLIW (very-long-instruction-word)-styled architecture is available with a datapath-functional resource library and a number of preconfigured microarchitectures with varying parallelism and performance. OptimoDE Data Engines are AMBA (Advanced Microcontroller Bus Architecture)-compliant and are compatible with ARM's DSP interface specification, which describes the interfaces between the cores for mailbox-based command and control messaging and bulk data passing, debugging and trace interfaces and protocols for multicore debugging, and software APIs for interprocessor communications. You can use OptimoDE as stand-alone processors or in designs with microprocessor cores.

ARM's Versatile Platform FPGA environment supports OptimoDE data engines. The tool environment enables the de-



signer to configure and extend the type and number of datapath-resource units and configure the size and topology of local storage and the level of interconnect. The C compiler and profiling-analysis tools support programming the OptimoDE data engines in C or C++. The tool environment automatically generates simulation models to assist in verifying the integration process of the data engine within a system design.

### CAMBRIDGE CONSULTANTS

Cambridge's APE2 configurable-VLIW (very-long-instruction-word) core targets low-end SOC (system-on-chip)/ASIC applications. A typical 16-bit configuration uses as few as 7000 gates. APE2 features a parallel structure with processing modules, such as single-cycle MAC (multiply-accumulate) units and ALUs connected to a common data-routing bus. Designers configure the DSP for the application by choosing the appropriate processing-module functions and quantities from the library and configuring the width of the data bus in increments as small as a bit at a time. The APE2 uses separate buses for instruction ROM, data RAM, and I/O registers, allowing simultaneous operation on each bus and single-cycle execution. Shared memory, shared registers, or both provide the interfacing to standard micro-controllers.

APE2's data-routing bus allows the output of any processing module to be available at the input of any other, and it allows the datapath connection or connections to change instruction cycles. Dynamic datapath routing and hardware configurability allow designers to implement signal-processing and control algorithms on a small die. APE2's library of processing modules includes MAC, ALU, FFT, Cartesian-to-Polar conversion, sequencing, I/O registers, and memory interfaces. Special instructions include coordinate transforms, digital quadrature oscillator, and radix-4 butterfly. Designers may also include custom-processing modules.

APE2 licensees have access to a development-tool suite that supports hardware selection; code generation for any hardware configuration; optimization analysis, including code compression; and software simulation. The tools automatically generate Verilog source code, including ROM-decompression hardware. You can perform verification between The Mathworks' ([www.mathworks.com](http://www.mathworks.com)) Matlab models, the APE2 software simulator, the Verilog simulator, and the target ASIC-hardware implementation via a common debugging-trace capability.

video and audio processing; VoIP (Voice Over Internet Protocol) gateways; broadband modems; and home entertainment, including digital TV, HDTV, PVRs, and DVDs. The Ceva-X architecture uses a mix of VLIW (very-long-instruction-word) and SIMD (single-instruction-multiple-data) architectures to provide a high level of concurrent instruction processing and to reduce code size. Support for dynamic- and selective-unit shutdowns and variable-clock speeds support low power consumption.

Ceva-X offers a scalable computation architecture for two-, four-, and eight-MAC systems. Each MAC unit is part of a computation cluster that includes a dedicated register file with additional logical, arithmetic, and bit-oriented mechanisms. Other scalability dimensions are 16- or 32-bit data-word width and the type of data and program memories. The Ceva-X architecture supports custom-defined instructions and function extensions that can use the internal DSP resources. The compiler-driven Ceva-X architecture implements an orthogonal instruction set, a load/store architecture, byte addressing, and a simple memory configuration that includes no X/Y partitioning.

Instructions can operate on 40-bit, 32-bit, 16-bit, and 8-bit data types. The SIMD capability allows a single instruction to operate on two-word or 4-byte packed data within a single accumulator. Ceva-X special instructions include FFT pointer post modifications, absolute difference, powerful average, multiply and multiply-accumulate of bytes, Viterbi support, and insert and extract. All instructions are conditional based on a set of predicate registers, which reduces the need for branches.

The Ceva XpertMedia digital-media platform targets cellular, consumer, and home-entertainment applications and comprises the Xpert hardware platform, the Xpert software framework, and the digital-media software. The Xpert hardware platforms are open DSP subsystems that include a DSP core with DSP-related peripherals and system interfaces, such as DMA controller, timers, serial ports, and parallel ports. Currently, the XpertMedia supports the XpertTeak. The Xpert software framework comes in both stand-alone-DSP and DSP and RISC configurations. It includes an RTOS, drivers, and messaging that combine with development tools and a host emulator. It provides a standard environment for DSP-software development

by using an Xpert DSP for multiple functions and applications. The digital-media software set of industry-standard video codecs includes JPEG, MPEG-4, MPEG-2, and H.264 as well as audio codecs, such as MP3, AAC (Advanced Audio Coding), AMR (adaptive multirate), and WMA (Windows Media Audio). The video-codec software uses the FST (fast-subspace-tracking) algorithm; Ceva's patented technology accelerates the basic elements composing a video codec by a factor of 20 to 200.

**CEVA** Ceva this year changed its name from ParthusCeva. It also changed the names of its DSP cores. PineDSP Core is now Ceva-Pine, OakCore is now Ceva-Oak, Teak DSP Core is now Ceva-Teak, TeakLite DSP Core is now Ceva-Teak-Lite, Teak DSP Core is now Ceva-Teak, PalmDSPCore is now Ceva-Palm, XpertTeak is now Ceva Xpert-Teak, and VOPstream is now Ceva Xpert-VoP. New cores include the Ceva-X, Ceva-X1620, and Ceva Xpert-Media.

Ceva-X1620 is the first implementation of the Ceva-X DSP family of cores comprising a 16-bit data width and two MAC (multiply/accumulate) units. The Ceva-X1620 targets 3G cellular handsets; software radio; smart phones and PDAs; mobile



The CW4512 builds on and replaces the CW4511 by adding I/O capabil-



ities, such as USB, LCD outputs, and triple DACs for NTSC or PAL outputs, targeting digital-camera applications. The CW4512 lets you implement a digital camera, including image-processing algorithms, memory control, and other house-keeping functions with one VLSI (very-large-scale-integration) chip. The CW4011 and CW4512 can achieve CIF (Common Intermediate Format)-level MPEG-4 encoding at more than 30 frames/sec, VGA-level encoding at 15 to 24 frames/sec, and JPEG compression at more than 20 million pixels/sec. This processor family includes special instructions for imaging, including a dot-product and a sum-of-absolute-differences instruction. The 16-bit video-in and -out ports with 256-byte FIFO buffers support simultaneous data transfers at 50M words/sec. The CW4512 includes integrated PWMs for motor control and a dedicated port for SD (secure-digital) flash-card storage.

ChipWrights can provide the Metrowerks' ([www.metrowerks.com](http://www.metrowerks.com)) CodeWarrior integrated development environment for the CW4011 and the CW4512. These tools include an assembler, ANSI C and C++ compilers, a linker, a simulator, and a profiler in an integrated, easy-to-use package. ChipWrights also provides a near-production-ready camera-reference design that implements a combined digital-still/digital-video camera using JPEG and MPEG-4 compression. This referenced design comes with a full development package that includes integrated firmware, schematics, bills of materials, and sample boards.

## CIRRUS LOGIC

The CS49500, Cirrus Logic's newest audio-DSP family, relies on dual 32-bit DSP cores for audio applications, with dual-MAC (multiply/accumulate) units and 72-bit accumulators for decoding and 96-kHz, multichannel postprocessing. The CS49500 family of single-chip devices requires no external RAM to support all industry-standard decoding algorithms, such as Dolby Digital-Pro Logic IIx, DTS-ES 96/24 with THX, and customer-programmable algorithms. The CS49500 family has enough ROM to store all mainstream application codes and supports extension to future algorithms via external downloading of code into RAM. The CS49500 family includes the dual-decoder CS49520, which can simultaneously decode DTS and Dolby Digital, or AAC and Dolby Digital. The dual-core architecture can operate as two separate 32-bit DSPs with different clock domains. Dual decoding, an advanced feature, enables new AVRs (audio/video receivers) to support dual zones with content coming from two sources.

The CS49500 comes with development tools, including a C compiler, an assembler, a linker, a simulation environment, and a real-time debugger. Cirrus provides reference designs, such as home-theater systems. The DSP AVR reference design includes a library of firmware for feature differentiation. Cirrus maintains an up-to-date product Web site containing product literature; descriptions of products; related documents; and design resources, such as application notes, evaluation boards, and users guides.

## CLARKSPUR

All emulator boards now support USB-cable controls, and Clarkspur is offering license-free audio-compression programs, such as OggVorbis.

## CRADLE TECHNOLOGIES

Cradle Technologies' CT3400 multiprocessing DSP contains a scalable multiprocessing RISC and DSP architecture in a single device. The CT3400 contains eight 32-bit DSPs, each with its own dedicated local-instruction memory. The instruction set includes SIMD (single-instruction-multiple-data) and support for sum of absolute difference. Each DSP contains an optimized DSP MAC (multiply/accumulate) unit, which allows the CT3400 to perform 128 8×8-bit multiplications per cycle or 32 16×16-bit multiplications per cycle. Each DSP supports fixed- or floating-point operation and can perform fixed- and floating-point conversion with no performance degradation.

The CT3400 also contains six RISC-like CPUs to perform system control and computation. The 192 kbytes of on-chip memory and a three-level memory-bus hierarchy simplify memory transfers between processors and remove traditional bottlenecks. The three levels include dedicated memory for each DSP, shared memory between the DSPs and RISC CPUs, and external SDRAM. An internal, 64-bit, 330-MHz global bus connects the shared memory and external SDRAM. A dedicated, 64-bit, 133-MHz interface provides access to the SDRAM. Three 32-bit, memory-transfer, DMA-like CPUs access the global bus to efficiently move data.

The CT3400 uses a software-programmable I/O subsystem, which includes two of the six RISC-like CPUs with local memory and DMA capabilities and pin-oriented PLAs and data FIFOs. Software-defined I/O functions include interfaces, such as a 10/100-Gbit Ethernet MAC unit; 33-bit, 33-MHz PCI; CCIT 601/656, flash memory; and custom interfaces. The CT3400 operates at 1.2V for the core and 3.3V for the I/O. The company fabricates it on a 0.15-micron, seven-layer, metal-CMOS process, and it is available in 230- and 260-MHz speeds.

Version 4.1 of the Cradle rapid-development system includes an integrated software-development kit that operates on a PC and supports Windows 2000, Windows XP, and Windows NT operating systems. Front-end tools include a full GCC-compliant C compiler (with Gnu libraries) and a Cradle DSP assembler. The application profiler includes memory-access tracking for DSP and RISC local memories and external DRAM. The software-development kit includes a cycle-accurate simulator. An optimized version of the open-source eCOS operating system supports multithreaded operations that you can mix with native multiprocessing operations that the CT3400 devices support. The debugger enables rapid switching between the simulator and the target hardware, and it supports concurrent debugging of all the RISC and DSP processors under one user in-



terface. You can access every register on every processor from the debugger. Multiple hardware breakpoints are available, and you can trigger them based on myriad conditions. Hardware-based single stepping supports debugging on any processor or any number of processors.

Hammerhead, a video-phone/conferencing reference design, incorporates an H.264 video codec and a G.729AB audio codec with IP (intellectual-property)-transport algorithms with onboard Ethernet and physical ports for both video in/out and audio in/out using a single CT3400 device. Barracuda, a network-videocamera application, incorporates interfaces to camera and CCD input, optional video preprocessing, a flexible choice of video encoder for compression, and IP transport using a single CT3400 device. IP-algorithm releases for the CT3400 include video/image codecs, including JPEG, MJPEG, H.264, and MPEG-4; audio codecs, such as G.711 and G.729AB; image processing, including Bayer interpolation, color conversion, and scaling; and IP transport. IP-interface releases include 10/100 Ethernet MAC, CMOS image sensor, PCI, and 656/601 video interface.

**DSPFACTORY** Dspfactory's application-specific Toccata Plus reconfigurable DSP system targets use in audio, such as digital-hearing-aid applications, in which sound quality, power consumption as low as 400  $\mu$ A at 1.25V, and miniaturization are critical design requirements. The 16-bit DSP core and 18-bit WOLA (weighted-overlap-add) filter-bank coprocessor, which executes time- and frequency-domain transforms and other vector-based computations, support adaptive-signal-processing schemes for wide dynamic-range compression, noise reduction, adaptive directional processing, and adaptive feedback cancellation. The audio-processing system includes two 16-bit ADCs, two 16-bit DACs, and two on-chip direct-digital-output drivers that enable the use of zero-bias receivers and eliminate the need for Class D receivers. Toccata Plus includes multiple analog/digital inputs and outputs to interface with a variety of transducers, switches, potentiometers, and other devices for hearing-aid designs, from the tiniest CIC (completely in-canal) models to full-featured BTE (behind-the-ear) models.

The high-performance, programmable BelaSigna 200 mixed-signal DSP-audio system targets digital-speech and audiocentric applications, such as Bluetooth wireless headsets, industrial and specialty headsets, and hands-free car kits. The BelaSigna 200 combines the 16-bit, software-programmable Rcore DSP core and the WOLA filter-bank coprocessor to provide a complete audio-processing chain. The analog portion of the system includes two 16-bit ADCs and two 16-bit DACs. The two on-chip direct-digital-output stages allow BelaSigna 200 to directly drive output transducers, eliminating the need for external power amplifiers. Algorithm-software support includes a Bluetooth SBC (subband-codec) encoder/decoder, noise reduction, echo cancellation, voice command, voice prompts, proprietary low-bit-rate speech coders, speech en-

hancement, and SRS (Sound Retrieval Systems) Labs' ([www.srslabs.com](http://www.srslabs.com)) WOW/VIP (voice-intelligibility processor).

Dspfactory offers a suite of simulation, evaluation, development, and application tools for each of its devices. The WOLA toolbox allows developers to simulate Dspfactory's WOLA filter-bank coprocessor in a variety of environments with support for The Mathworks' ([www.mathworks.com](http://www.mathworks.com)) Matlab and C-language simulations. The SignaKlara block set provides a library of Dspfactory building blocks for users of The Mathworks' Simulink that facilitate algorithm prototyping in a drag-and-drop environment. This tool lets developers insert Dspfactory blocks within their own Simulink-algorithm model and simulate the capabilities and performance of the WOLA filter-bank coprocessor and SignaKlara firmware routines.

### LSI LOGIC

LSI Logic has added to its product offerings a low-cost core, the ZSP200, and two DSP cores, the low-power ZSP500 and the high-performance ZSP600, that are based on the G2, second-generation, instruction-set architecture. The ZSP200 single-MAC (multiply/accumulate)-unit core derives from the ZSP400, and it is half the size and uses half the power of the ZSP400. The G2 instruction set is upward-assembly-code-compatible with the first-generation ZSP400 and has 16 or 32 variable-length instructions, enhanced stack support, enhanced bit manipulation, and multiply/add instructions that mimic ANSI-C function calls. The ZSP500 and ZSP600 cores support instruction extensibility, allowing designers to add as many as 256 custom instructions via a coprocessor interface. Last year's directory contains more information on the ZSP500 and ZSP600. LSI Logic's ZSP Division offers the ZSP200, ZSP400, ZSP500, and ZSP600 cores as standard products; ASIC hard macros; and licensable, synthesizable RTL (register-transfer-level) logic. ARM's Realview tools platform now supports ZSP development.

An evaluation and development kit includes an evaluation/development board for rapid prototyping, evaluation, and testing; sample code demonstrating real-time algorithms; bundled UltraEdit advanced and integrated development editor with Dspfactory extensions; firmware support, including the BAT (basic-algorithm tool kit) for developing real-time algorithms; a complete compilation-tool chain, including a C pre-processor, an assembler, a linker, and a librarian; enhanced tools for developing algorithms, including low-level debugger and EEPROM-manager-layout tool; and documentation.

**MOTOROLA** The 56F8300 family of devices can execute code from Motorola's third-generation flash memory as fast as 60 MHz without using any acceleration technology. The family provides 32 to 256 kbytes of on-chip flash program memory and the ability to support as much as 32 Mbytes of off-chip memory. The 56F8300 devices support an operating range of  $-40$  to  $+125^{\circ}\text{C}$ , and they offer flash protection and security. Similar to the 56F800 series, a small page in the flash memory supports EEPROM emulation. The 56F8300 series of devices targets automotive, instrumentation, and industrial-networking applications, including electronic



power-assisted steering, hybrid braking, and data-acquisition and factory-automation systems.

Motorola also added two devices, the 30-MIPS 56F801FA60 and the 56F802TA60, to the 56F800 product line. They are variants of the 40-MIPS 56F801FA80 and 56F802TA80 and are available in 32- and 48-pin packages targeting industrial fans, compressors, exercise equipment and control pumps.

A new, single integrated development environment from Metrowerks ([www.metrowerks.com](http://www.metrowerks.com)) supports development for all Motorola 56800/E based products. Complimentary versions of the Metrowerks ([www.metrowerks.com](http://www.metrowerks.com)) tools are available with one-year maintenance for memories as large as 16 kbytes. You can upgrade the compiler to 32 or 64 kbytes or larger programs. The processor-expert RAD (rapid-application-development) tool provides autocode generation for on-chip peripherals and includes standard libraries for signal processing, software services, sample applications, and RTOS support. Motorola offers processor-evaluation boards, demonstration kits, and reference designs for motor control, hands-free car kits, automotive electronic braking and steering, power supplies, and energy management.

#### PHILIPS SEMICONDUCTORS

Philips based the Nexpria PNX1500 on a 32-bit TriMedia core with application-specific multimedia and floating-point instructions that target audio and video applications. The PNX1500 integrates a TFT (thin-film-transistor) LCD controller and Ethernet 10/100 MAC (multiply/accumulate) support. It can support real-time encoding and decoding of MPEG-2 or MPEG-4 (SP, MVP), MPEG-4 ASP decoding, DV decoding, H.263 encoding and decoding, DivX-5 decoding, MP3 encoding and decoding, AAC (Advanced Audio Coding) encoding and decoding, TCP/IP (Transfer Control Protocol/Internet Protocol), Ethernet, and Universal Plug 'n' Play.

The PNX1500 software-development environment supports C and C++ programming and includes application libraries for audio and video codecs. The Streaming networks NREF-1500 developer kit includes a board with a USB interface that you can use in a hosted or a stand-alone environment. A PCI-standard 2.2 host interface is available for hosted applications. The NREF-1500 development kit includes device drivers, test algorithms, and software samples.

#### RC MODULE

The 128-bit, high-performance 1878BM3 DSM (digital-signal memory) VLIW (very-long-instruction-word), accumulation and signal-processing SOC (system on chip) targets radar and sonar applications. It integrates two 6-bit ADCs supporting 600M samples/sec, four 8-bit DACs supporting 300M samples/sec, and eight DMA channels. The 2 Mbytes of on-chip SRAM allows the receiving and storing of high-frequency analog signals as long as 655  $\mu$ sec. The instruction set supports programmable amplification of input signals, summation with output signals,

a programmable Doppler shift, and as many as four concurrent on-chip memory load/store memory accesses. The 64-bit external bus provides fast instruction and data transfers in DMA and in random-access mode.

The NeuroMatrix MC431 single-DSP PCI-evaluation board supports software evaluation and system prototyping on a NM6403 DSP. It has one NM6403 DSP, 4 Mbytes of SRAM, and two communication ports. The NMPL (NeuroMatrix processor library) supports vector- and matrix-data operations on the NM6403 processor. The library functions use a C++ interface. RC Module implements most of the library functions on the vector core for the NM6403 processor architecture. For application-program development, the library has implementations of functions for x86 processors in C++ that allow designers to execute application programs written using this library on a PC.

#### SENSORY

The single-chip, mixed-signal SVC-64 targets voice-biometric applications, and it includes a microphone preamplifier, an ADC, a DAC, RAM, 16 general-purpose I/O lines, a 4-MIPS dedicated processor, and 64 kbytes of optional on-chip ROM. The SVC-64 has an 8-bit, variable-length-instruction processor core with an instruction set that is similar to that of the 8051 family of microcontrollers.

The SVC/SVC-64 processor uses symmetrical source and destinations for all instructions. The 2.5 kbytes of internal SRAM are organized as 2 kbytes of data space and 0.5 kbytes of register space. You can apply all arithmetic instructions to any register. You can use any pair of adjacent registers at an even address as 16-bit pointers as either the source or the destination for data movement. Instruction classes allow the pointer to access internal or external code space, internal registers, or external data space.

The SVC-64 supports the Voice Lock technology library, which focuses on voice-biometric-security applications. The SVC-64 development tool kit includes the voice-lock-technology library, demonstration units, and prototyping modules. Each kit includes hardware and software, documentation, and examples. Turnkey product-development and linguistics services are available directly through Sensory or through its worldwide network of third-party-development houses.

#### STARCORE

StarCore now offers a fully synthesizable 2- and 4-MAC version of the StarCore core. The 2-MAC configurations include the SP1201, SC1202, and SP1203, and the 4-MAC versions are the SP1401, SP1402, and SP1403. StarCore offers customers a one-week performance evaluation to provide details of what they can expect in performance, including frequency, operation power, power dissipation, and chip size, based on the customer's selection of foundry process, memory configuration, and StarCore processor platform. Customers receive the written report within one week.

StarCore has expanded its alliance of third-party-tool providers to include Metrowerks ([www.metrowerks.com](http://www.metrowerks.com)), Green Hills ([www.ghs.com](http://www.ghs.com)), TTPCom ([www.ttpcom.com](http://www.ttpcom.com)),



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Lyrtech ([www.lyrtech.com](http://www.lyrtech.com)).

## TENSILICA

New this year for Tensilica is Xtensa Xplorer, an integrated design environment for SOC (system-on-chip) development that integrates software development, processor optimization, and multiple-processor-SOC architecture tools into one environment. Tensilica based the Xtensa Xplorer IDE in part on the open-source Eclipse platform for tool integration. The Xplorer IDE allows designers to simultaneously design both the hardware and the software, make trade-offs for processor configurations, and track projects. Xplorer serves as a cockpit for basic design management and invocation of Tensilica software-development and processor-configuration tools, such as the Xtensa processor generator and the TIE (Tensilica-instruction-extension) compiler.

Xplorer provides a unified environment for C and C++ application-software development, C and C++-program debugging, code profiling and visualization, and SOC configuration management for designing multiple Xtensa processors into a system. Xplorer includes a context-sensitive TIE-source-code editor, a TIE-instruction-aware debugger, and a gate-count estimator. The gate-count estimator gives real-time feedback to software designers unfamiliar with gate-count implications of hardware development.

Tensilica provides support for application-optimized Xtensa configurations for operating systems and IDEs from Accelerated Technology ([www.acceleratedtechnology.com](http://www.acceleratedtechnology.com)), MontaVista ([www.mvista.com](http://www.mvista.com)), and Wind River ([www.windriver.com](http://www.windriver.com)). Xplorer complements these integrated development environments by providing Xtensa-specific productivity and analysis enhancements earlier in the SOC-design process.

network videocamera applications. The TMS320DM640 and TMS320DM641 processors also target video-client type applications, such as IP-based video recorders, set-top boxes, security surveillance, and network cameras. The VSIP development platform includes TI's Code Composer Studio Version 2.2 integrated development environment, the Quartus II programmable-logic development environment, TI's XDS560-class emulator, and documentation. The development platform includes embedded software for audio/MPEG-4-SP video-compression libraries, application-oriented algorithms, application-sample source code, and a PC-supervision application to decode and control the embedded platform. The TMDSVSK642 VSIP is available for NTSC and PAL development with or without the Ateme emulator.

TI based the TMS320C5509A fixed-point DSP on the TMS320C55x DSP core, a highly integrated DSP that includes full-speed USB; a 10-bit ADC; and Multimedia Card, Secure Digital, and Sony memory-stick serial interfaces targeting portable and connected handheld devices. The Analysis tool kit for TMS320C5000 DSP platforms provides increased application visibility and the opportunity to profile and model full-DSP applications. The Analysis tool kit includes new on-chip-cache-memory-conflict, pipeline-stall, and code-coverage analyzers and a new multievent function profiler.

Texas Instruments jointly announced with Clarity Technologies ([www.clarity.com](http://www.clarity.com)) the HFK (hands-free-kit) development platform, which includes a hardware platform and real-time voice- and audio-enhancement algorithms targeting cellular aftermarket accessories. The HFK development platform is based on the C5000 DSP platform and connects to TI's Code Composer Studio development tools through a JTAG connection. The HFK development platform includes a TMS320C5407 DSP motherboard, CVC Blue acoustic-echo-cancellation and noise-reduction software from Clarity Technologies, library samples, documentation, a power supply, a line out, an onboard microphone, a 2.5-mm microphone jack, a JTAG connector, three LEDs, and three pushbuttons.

The C2000 group introduced the TMS320F2801, F2806, and F2808 flash-based digital-signal controllers, which target embedded-control applications, such as automotive, industrial, and white-good appliances. The new controllers include event managers, ADCs, and on-chip flash memory. TI based the new TMS320C2812, C2811, C2810, and TMS320F2811 controllers on the control-optimized TMS320F28x core; they feature ROM. The TMS320F2811 offers 150 MIPS of control performance with 128k words of flash memory in an LQFP. The DMC550 motor-development-board drive platform for brushless-dc motors allows you to develop and implement your code on TMS320C24x controllers. The DMCLib (digital-motor-control library) of motor-specific algorithms covers one- and three-phase, sensed and sensorless, and ACI (ac-induction), BLDC, PMSM (permanent-magnet-synchronous), and SR (switched-reluctance) motors. The stand-alone TMS320LF2407A eZdsp platform for the TMS320LF2407 fixed-point

## TEXAS INSTRUMENTS

The general-purpose VLIW (very-long-instruction-word) TMS320C6414T, C6415T, and C6416T DSPs offer processor speeds as high as 1 GHz at 90 nm. The DSPs provide eight billion MACs (multiply/accumulates) on 8-bit data for video and imaging applications or four GMACs on the 16-bit data common to speech and audio applications. This performance enables these DSPs to target adaptive-antenna-array, smart-car, and artificial-vision applications and increases the bandwidth and channel capacity of applications, such as wireless base stations, Internet Protocol-based video, high-speed broadband networking, medical diagnostics, and radar.

Texas Instruments jointly announced with Ateme ([www.ateme.com](http://www.ateme.com)) the availability of the VSIP (Video Security over Internet Protocol) development platform, based on TI's TMS320DM642 digital media processor, targeting intelligent-



controller has an embedded parallel port/IEEE 1149.1 scan controller to support true-JTAG emulation. The eZdsp has 32k words of external program and 32k words of external data-memory operating at zero wait states.

Texas Instruments has added Linux development tools and support for the OMAP5910 embedded processor. TI increased simulation speeds as much as 21 times over previous offerings.

## XILINX

Xilinx offers FPGAs, such as the Virtex-II Pro and Spartan-3 families, which can complement DSPs by providing signal-processing acceleration, bus bridging, and system-logic consolidation. These devices include an array of 18×18-bit embedded multipliers that is useful for implementing highly parallel datapaths, block and distributed memory that is useful for vector-based processing or storing data or coefficients, and SRL (shift-register logic) 16 that can increase the computational density of multichannel datapaths. The Virtex-II Pro devices include as many as 566 18×18-bit embedded multipliers, as much as 10 Mbits of block memory, as much as 2 Mbits of distributed memory, and as many as 125,135 SRL16 elements. The Virtex-II Pro can also include as many as four embedded PowerPC cores and multiple MicroBlaze or PicoBlaze soft-processor cores. The

Spartan-3 devices include as many as 104 18×18-bit embedded multipliers, as much as 1.9 Mbits of block memory, as much as 520 kbits of distributed memory, and as many as 74,880 SRL16 elements. The Spartan-3 can also include multiple MicroBlaze or PicoBlaze soft-processor cores.

Xilinx provides DSP algorithms, such as filters, math functions, transforms, DDCs (digital downconverters), DUCs (digital upconverters), and correlators, as part of the Xilinx Integrated Software Environment that designers can implement as IP (intellectual-property) cores. Optional licensable cores include Reed Solomon encoders and decoders, Viterbi decoders, TPC (turbo-product-code) encoders and decoders, interleavers and deinterleavers, TCC (turbo convolutional code) for the CDMA2000, and DOCSIS J-83 modulators. Additional IP cores are available from Xilinx AllianceCore partners. The DSP-design tools include the System Generator for DSP for generating HDL or bit streams from The Mathworks' ([www.mathworks.com](http://www.mathworks.com)) Simulink. It supports hardware in the loop using JTAG, HDL cosimulation, system debugging at operating speeds, AccelChip for The Mathworks' Matlab to RTL for Xilinx FPGAs, and CoWare SPW (signal-processing work system) for targeting Xilinx FPGAs. Xilinx also offers educational services. □

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