Module®

RESEARCH CENTRE

# COMPANY PROFILE

Founded

1990

Number of employees

650

- Integrated Circuit Design (microelectronic design services),
- Design and manufacture of special computational modules, control systems for special applications (onboard and aviation equipment)
- Production and design of video recognition and analysis systems (DSP)
- Introduction of neural networks in modern automated complexes of various industries: from navigation and radar to unmanned vehicles and robotics


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# NEUROMATRIX® ARCHITECTURE

1995 - Module has started development of NeuroMatrix® architecture. The architecture is optimized for matrix multiplication algorithms and capable of dynamic precision and performance.

- A specific feature of this architecture is an authentic high-performance vector-matrix coprocessor
- The efficiency of the matrix multiplication operation is close to the theoretical peak
- Low power consumption allows the NeuroMatrix® processors to be used in embedded devices for emulation of deep convolutional networks
- 4 generations of NeuroMatrix® architecture implemented
- The latest generation (NMC4) featuring hardware support of floating-point computation

nmDL software package (Neuro Matrix for Deep Learning) has been developed to apply the trained deep neural networks on the NeuroMatrix® platform (TensorFlow® or Caffe® libraries).

>15

IP certificates for NeuroMatrix® processor software

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# Russian NeuroMatrix® processors

1995 — 2019


NM6403 — NM6408

- Class - 32/64-bit RISC / DSP fixed and floating point
- Highest performance on vector-matrix operations (neural networks, processing of radar, video and signal data)
- Dynamically changing performance to bit ratio
- Patents of the Russian Federation, USA and Korea

## Main applications

Radar, video processing, neural networks, robotics, GNSS, SDR navigation and communications, astro-orientation, digital television, multimedia, etc.

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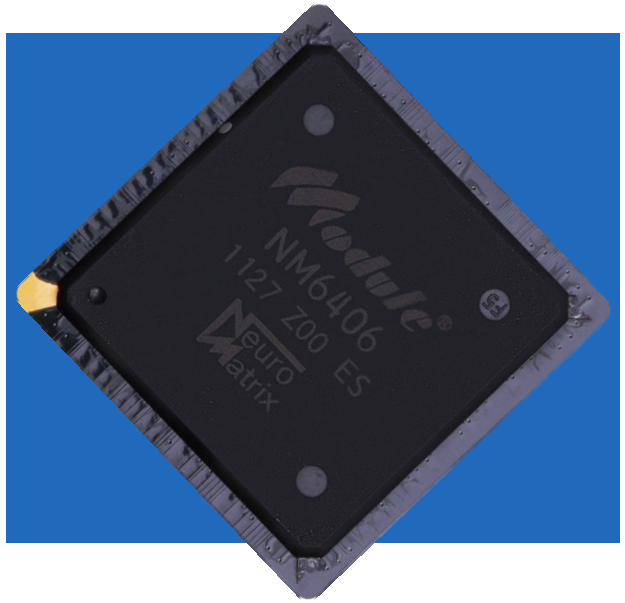


# NM6406

## High performance DSP processor

**NM6406** is a high performance DSP processor designed for real time data flow processing. The architecture is based on the advanced VLIW/SIMD NMC3 core, and consists of a 32/64-bit RISC processor and a 64-bit VECTOR co-processor. The co-processor supports vector/matrix operations with elements of variable bit length (US Pat. 6539368 B1)

## Features

CMOS technology
**90nm**

Package
**416 BGA**

Clock frequency
**320 MHz**

Power supply
**1,2 V (core) 3,3 B (I/O buffers)**

Power consumption
**less than 1,2 W;**

Performance
**320 MIPS (960 MOPS)**

Temperature range
**-55°C ... +85°C.**

## Applications

- IR and video processing
- Navigation
- CDMA и TDMA base station

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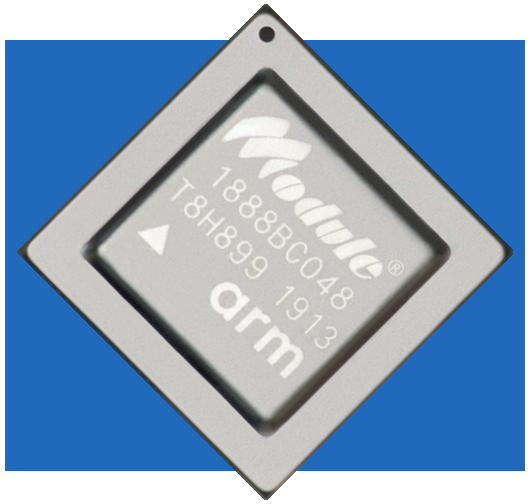


# 1888BC048

NEW

A versatile 32-bit processor with a wide range of interfaces.
Designed for use in embedded equipment.

## Features

CMOS technology
**28 nm TSMC**

Package
**HSFCBGA-676**

Processor Architecture
**ARM Cortex-A5**

Power supply
**0,9V (core)/3.3V (I/O buffers)**

Power consumption
**1.2 W**

Temperature range
**-60...+ 85 ° C**

## Applications

- General and real-time information control system:

as main SoC
as interface south bridge

- Ethernet NIC with embedded hypervisor, etc

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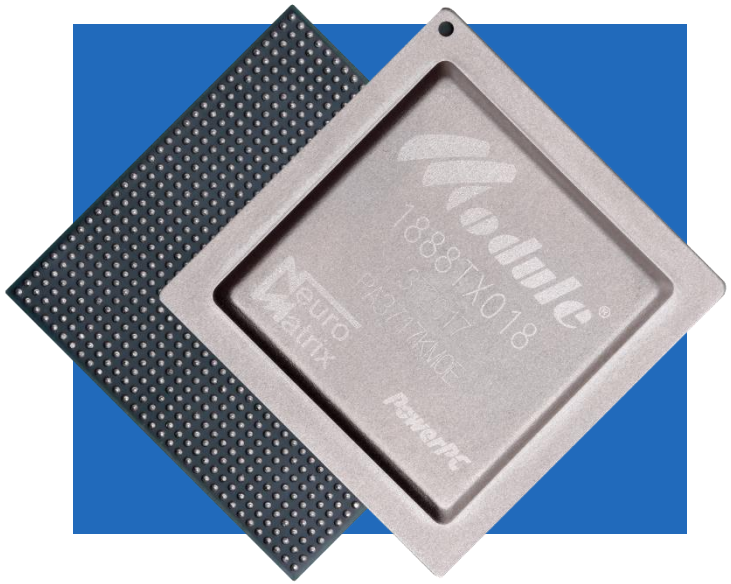


# MM7705

## HD Multimedia Processor

The chip is designed for use as a central processor for devices requiring high performance and high-energy efficiency in computing systems and devices for processing multimedia information.

CMOS technology
**28 nm**

Typical power
**8 W**

Maximum power
**15 W**

Processor Architecture
**PowerPC v2.05**

Processors
**2 CPUs (PowerPC 470S) and 4 DSPNMC3**

Power consumption
**Max 2,8W**

Hardware video encoder / decoder
**1080p high-definition, 60 frames per sec**

**DDR3 memory, 800-1600Mbps, 32 bits, 2 interfaces with the ability to connect up to 8 GB**

## Applications

- Onboard steering machines
- Input, output, processing, encoding / decoding multimedia information
- Switching and conversion of video streams

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# Neural Networks

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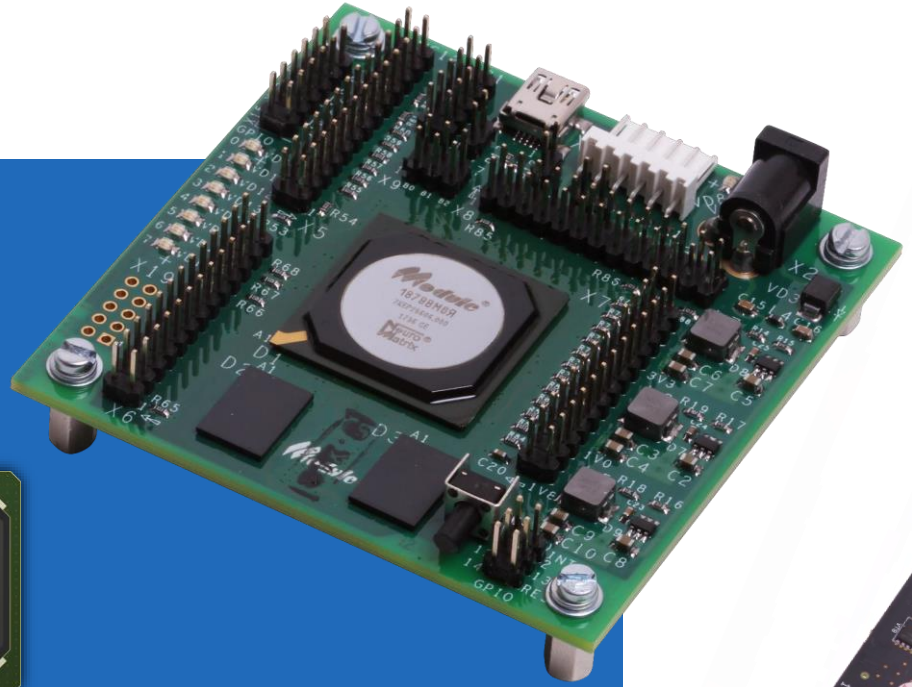
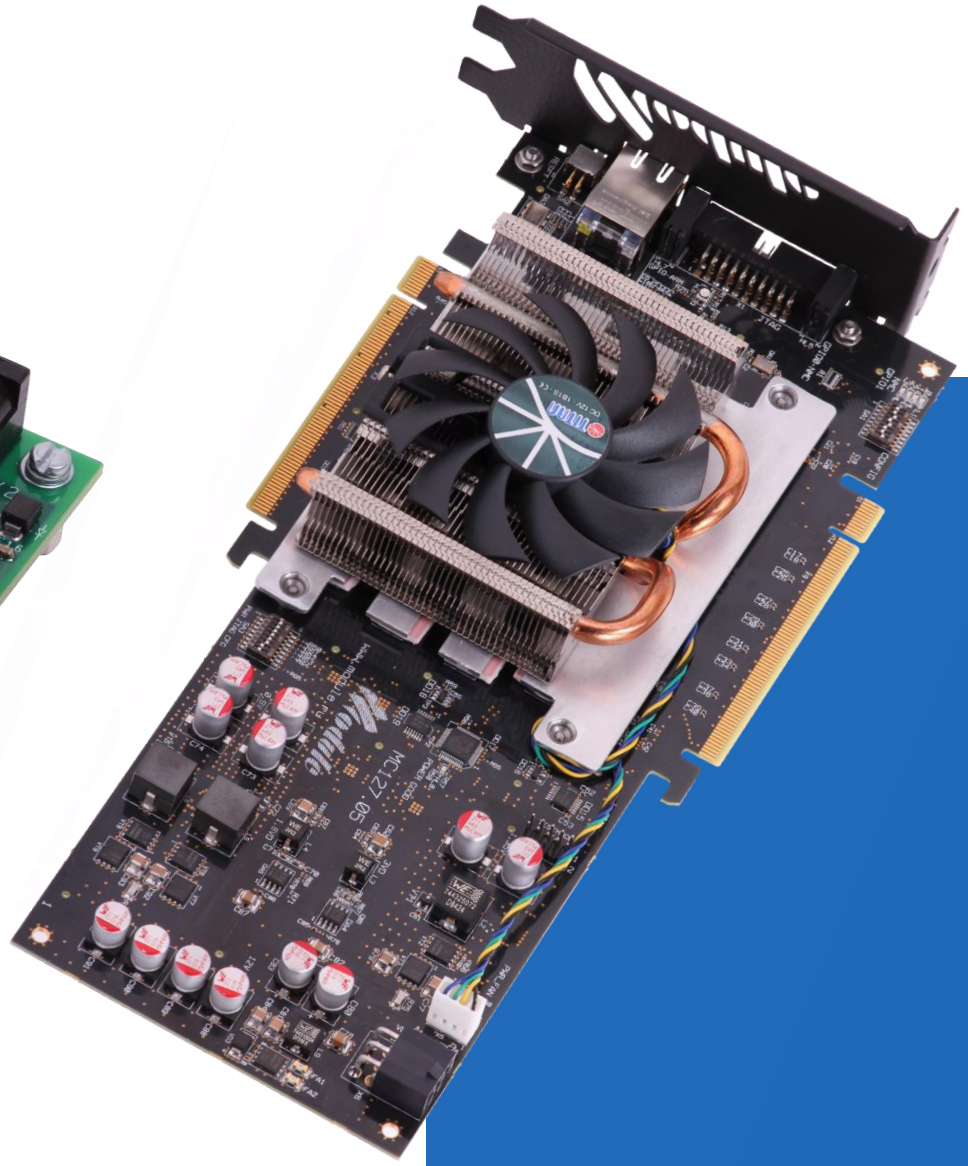
# NeuroMatrix neural network accelerators and computers

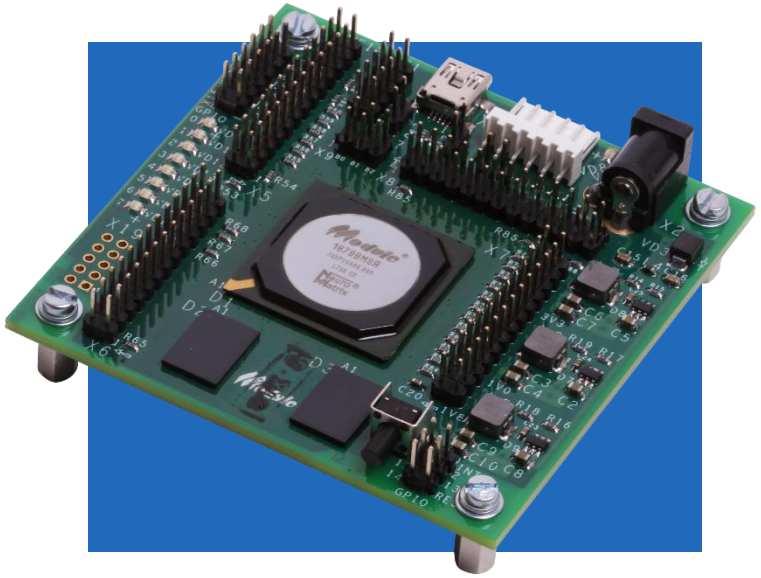



Embedded MC121.01 computer on the NM6407 processor




Neural network accelerator MC127.05 at NM6408 processor

Module RESEARCH CENTRE



# Neural Network Computer MC121.01

**MC121.01** is integrated circuit computer designed on the basis of a specialized neural microprocessor **NM6407**.
The module is designed to function as part of a complex, in particular with a PC with USB 2.0 interface. This module is designed to perform a wide class of tasks related to digital signal processing in real time.

## Features

Processor clock speed

**500 MHz**

Speed scalar operations

**Up to 500 million operations per sec**

The total amount of memory

**DDR2 SDRAM 512 MB**

Speed vector operations

**up to 12 billion operations per sec with byte operands**

Power consumption

**2.5 W**

Power supply

**5 to 12 V**

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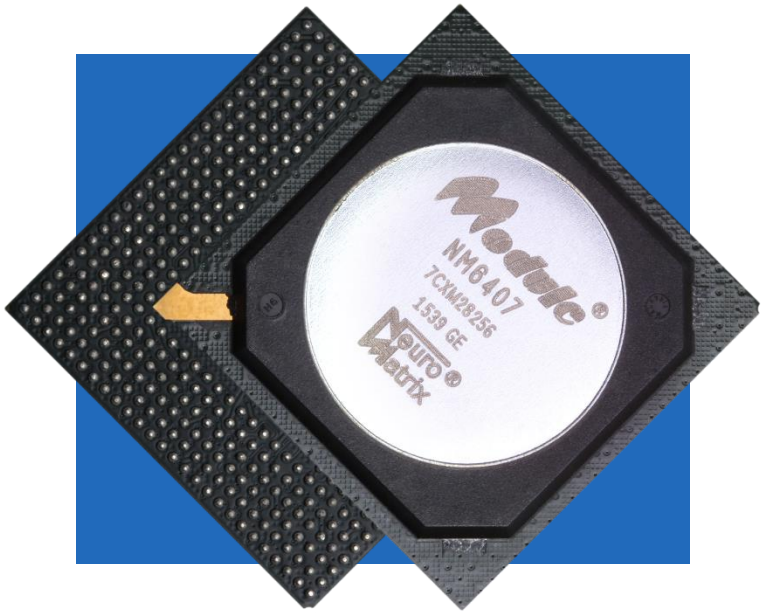


# NM6407

## High performance neuro-processor for DSP operation

The neuro-processor **NM6407MP** is based on **NeuroMatrix®** architecture combining the features of two architectures of VLIW / SIMD processors.
The chip contains two processor cores **NMPU0** and **NMPU1** with a RISC processor and a vector coprocessor for performing vector-matrix operations on integer data of variable length from 1 to 64 bits and floating point vector operations.

## Features

CMOS technology
**65nm**

Memory on a SoC
**16 Mbit**

Synchronization frequency
**500 MHz**

Voltages
**1.0V (core), 1.8V (DDR2), 3.3V**

Power consumption
**Typical 2.4 W**
**Max 7 W**

Performance
**16 GFLOPs**

Temperature range
**-45 ° C ... + 85 ° C**

## Applications

- Digital signal processing
- Navigation (transport)
- Radiolocation
- High performance signal switching CDMA and TDMA

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# Neural Network Accelerator MC127.05

The **MC127.05** is a **high performance computing module** with interface capabilities designed to be used as a universal hardware and software platform to receive, process, store and transfer large data in real time. The module can be applied as part of integrated systems to build a wide range of DSP and computer vision systems. The device is based on a heterogeneous high performance NM6408 neuroprocessor, consisting of 16 NM4 cores and five ARM Cortex-A5, five DDR3 controllers and a PCI-E2.0 interface.


## Features

- integrated circuit NM6408;
- 5 banks of DDR3 memory, with a total capacity of 5 GB,
- bandwidth up to 32 GB / s;
- PCIe2.0 x4 with a throughput of 4 GB / s;
- Ethernet 100 Mb/s (with EDCL support);
- High-speed communication ports with a capacity of up to 16 GB/s;
- microSD, GPIO (28 pins), JTAG;
- Power consumption - 15W;
- Power supply - 12V;
- PCIe x16 Form Factor, 2 Slots

## Applications

- Neural networks and artificial intelligence
- Specialized high-performance complexes
- Digital Signal and Image Processing Systems
- Machine vision systems
- Robotics

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# NM6408

## High performance neuro-processor

The universal neuro-microprocessor is designed for a wide range of tasks, especially in emulation of neural networks and deep learning for special purposes.

**NM6408** is capable of performing complex of operations connected with processing big data streams in real time: digital signal processing (DSP), image processing (recognition), navigation, communication, etc.

## Applications

- Deep Neural Networks
- SDR navigation and communication
- Video processing
- Radiolocation
- 3D computer vision
- Hybrid high-performance computing systems

## Features

| CMOS technology | Performance | Power consumption |
|---|---|---|
| 28 nm | 512 GFLOPs | 20W |

| Power supply | Package |
|---|---|
| 0,9V (core)/1,8V (I/O buffers) | 1444 HFCBGA |

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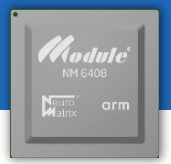
# NeuroMatrix Neural Network Ecosystem

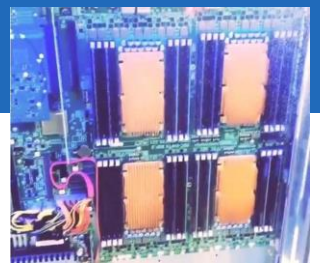
## Learning

NeuroMatrix®
NM6408




Neural Net Accelerator MC127.05

Supercomputer for neural networks training



Deep Learning Framework

## Inference

NeuroMatrix®
NM6407


Embedded Computer
MC 121.01

Tool software(SDK)

NMDL
NeuroMatrix®
Deep Learning

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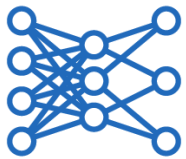
# Neuro Network Platform Key Elements

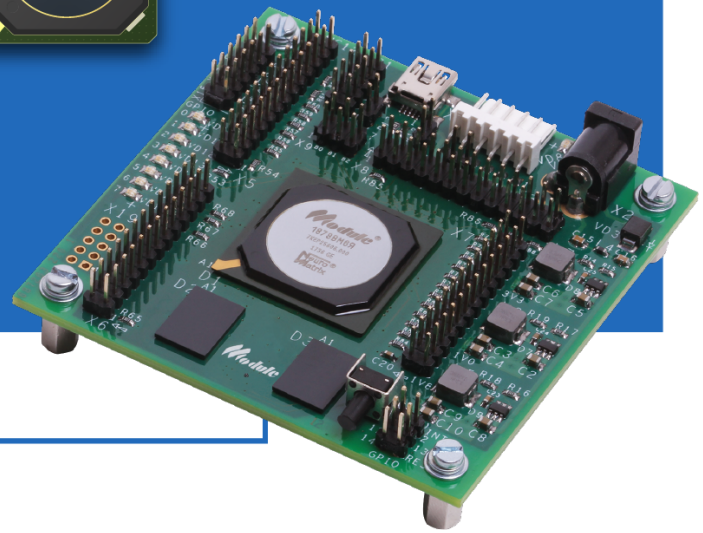
NeuroMatrix
**IP Core**


Neural Network
Accelerator
**MC127.05**

**NMDL (Neuromatrix® Deep Learning)**
a set of hardware and software for the development and implementation of deep neural networks on NeuroMatrix® processors




Neural Network
Computer
**MC121.01**



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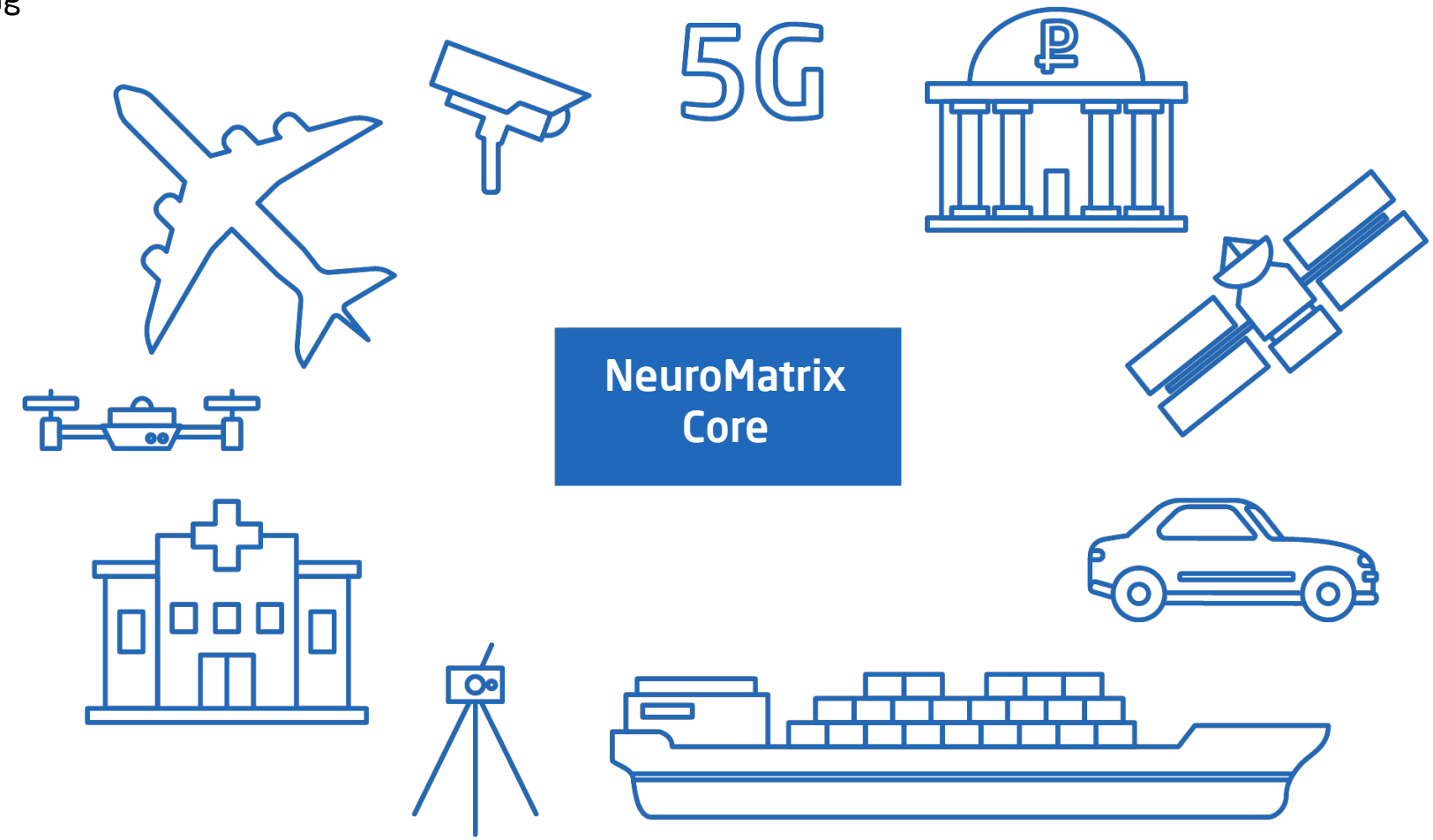
# NeuroMatrix Neuro Network Platform

Neural network training
(**Learning**)


NeuroMatrix®
NM6408

Neural networks implementation
(**Inference**)


NeuroMatrix®
NM6407




**Hardware and software systems:**

- **Telemedicine**
- **Smart transport**
- **Smart city**
- **Smart factories**
- **Drones**
- **Virtual reality**
- **Security systems**
- **Finance**

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# Operational Amplifiers

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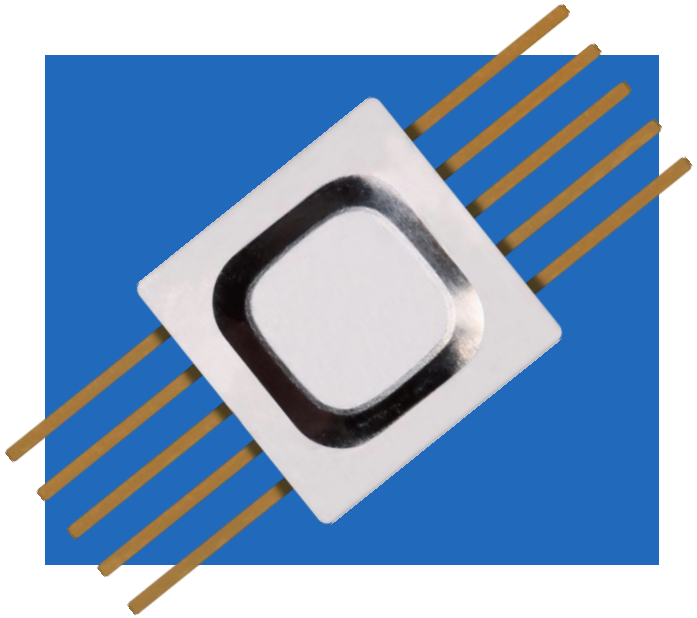

# OAVF1/OAVF2

**OACF1** - one-channel high-speed operational amplifier with voltage feedback.
**OACF2** - two-channel operational amplifier with voltage feedback.
Amplifiers provide high-dynamic accuracy in a wide frequency range and stable operating at gains up to AC = +1. The architecture of the input stages implemented on the bridge differential amplifier provides the **slew rate of the output signal and the cutoff frequency of the maximum power** previously achieved only in broadband amplifiers with current feedback.

OAs are used in schemes with deep negative feedback, which completely determines the gain / transmission coefficient of the resulting circuit. On the basis of OA it is possible to build many different electronic components.

## Features

Frequency
**210 MHz (AC = +2)**

Maximum output voltage
**7.2 V (U = ± 5 V)**

The slew rate of amplifier
**940 V / µs**

Output current
**130 mA**

Temperature range
**60 to +125 ° C**

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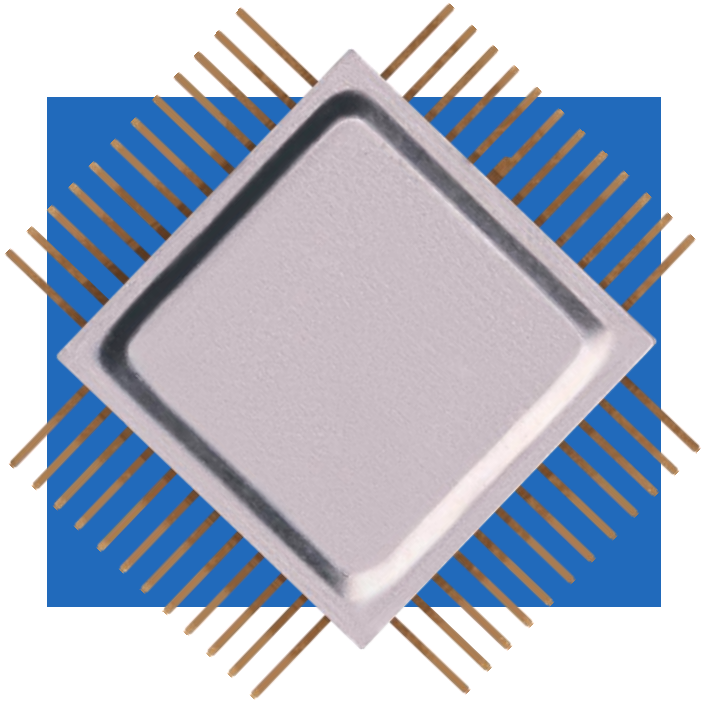

# 2OACF

## Two-channel operational amplifier (OA) with current feedback

It provides good dynamic parameters in a wide range of frequencies and gains, **stably operating on a low-impedance load with gains up to AC = +3 and RH = 10 ohms**. In the OS, the function of turning off each channel is implemented independently, which takes the outputs of the OA to a high-impedance state.
The OA is intended for use in the transceiver path of a high-speed multiplexed data transmission channel (MCPD).

## Features

Frequency

**240 MHz (AC = +4)**

Maximum output voltage

**7.6 V (U = ± 5 V)**

The slew rate of amplifier

**1030 V/μs**

Output current

**500 mA**

Temperature range

**60 to +125 ° C**

## Applications

- Analog-to-digital converters
- Digital-to-analog converters
- Current-voltage converters
- Voltage-current converters
- AC/DC

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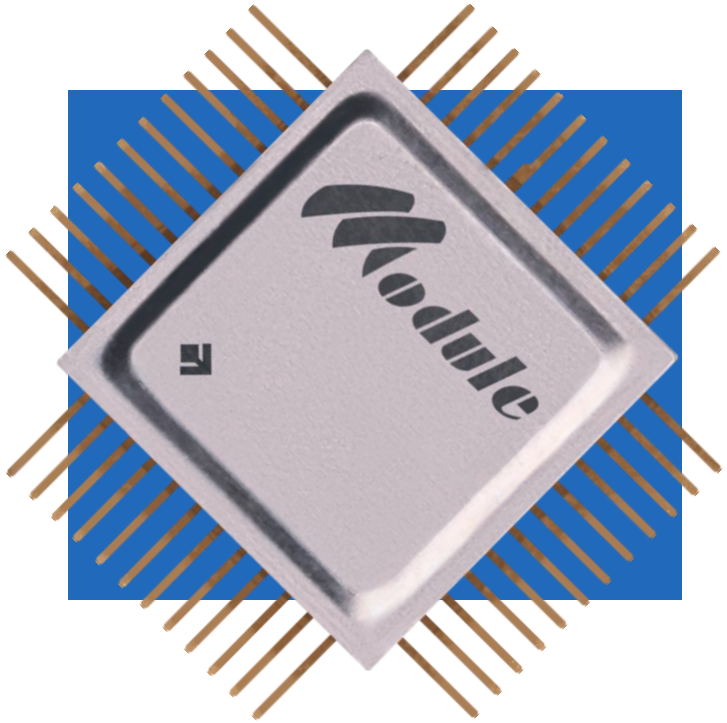


# 4OACF

## Four-channel operational amplifier (OA) with current feedback

It is designed for use in the transceiver path of the high-speed multiplex data channel (MDC). Two op-amp channels are designed for large output currents (up to 500 mA) for the transmitter unit. The other two are smaller (up to 130 mA) and are used for the receiver unit. Transmitter channels operate on a low-impedance load with gains up to AC = +3 and RH = 10 Ohm and have the function of shutting down each channel, independently transforming the OA outputs into a high impedance state.
The receiver channels operate at gains up to AC = +1.

## Features

Maximum output voltage

**7.6 V (UP = ± 5 V)**

The slew rate of amplifier

**1030 V / µs**

Frequency

**240 MHz (AC = +4)**

Output current

**500/130 mA**

Temperature range

**60 to +125 ° C**

## Applications

- Voltage comparators
- Differential amplifiers and integrators
- Voltage and current stabilizers
- Analog calculators and signal generators
- Analog-to-digital converters
- Digital-to-analog converters
- Current-voltage, voltage-current converters

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# Navigation

navimatrix by Module

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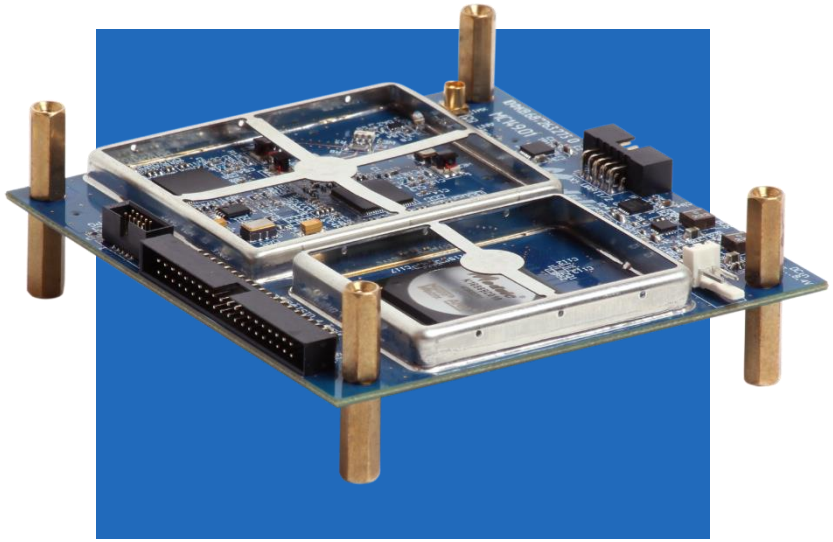

# GNSS RECEIVER MC149.01

**MC149.01** is a three-frequency receiver. It is designed to build **high-precision consumer navigation equipment** and provide **centimeter-level accuracy** in any kind of vehicles and automotive transport systems.
Compatible with library of high precision navigation RTKLib for work with **third-party** navigation equipment manufacturers.

Centimeter accuracy (1σ)

**in plan: 1 cm + 1 ppm**
**in height: 1.5 cm + 1 ppm**

Location Accuracy (1σ)

**offline mode: 2m**
**SBAS: 0.75m**

Simultaneous work in three frequency ranges

**GLONASS L1OF, L2OF, L3OC, GPS L1 C / A, L2CM, L5**

Hardware support

**BeiDou B1 / B2. Galileo E1 / E5a / E5b. QZSS L1 / L2**
**20Hz navigation solution temp**

Voltage

**3.7 - 8.4 V**

Power consumption

**1.6 - 1.8 W3**

## Applications

- **GLONASS / GPS / GALILEO / COMPASS**
- **Cellular signal receivers**
- **Digital broadcasting (DAB)**
- **Autonomous cars**
- **Robotics and drones**
- **Agriculture (precision farming)**
- **Geodesy**

navimatrix by Module

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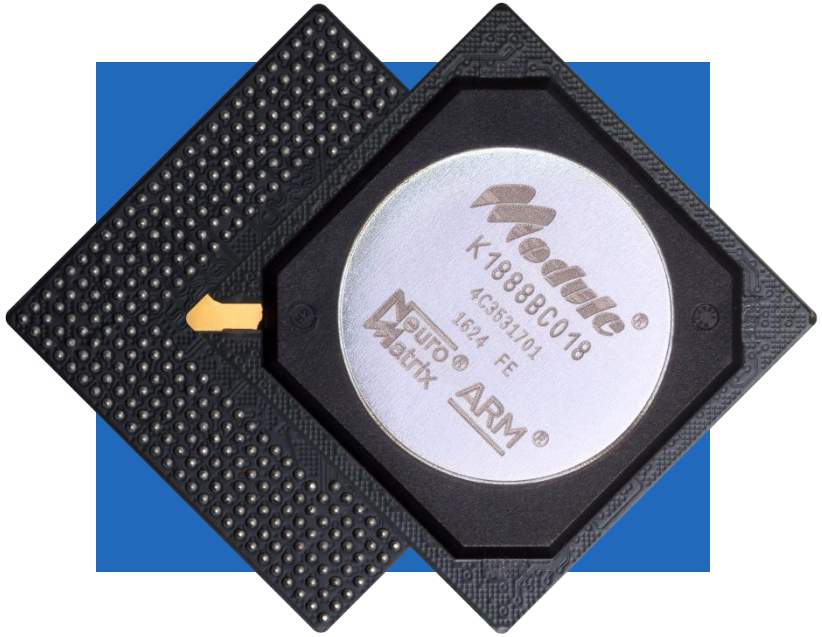


# BBP2

## High performance DSP processor (navigation)

The chip is designed for creating **high-performance measurement modules** that provide reception and processing GNSS GLONASS / GPS / GALILEO signals and SBAS functional add-ons in navigation equipment. It provides information on the integrity of the navigation field, corrects the information about the exact coordinates of the satellites and the time-frequency parameters of the system.

## Features

CMOS technology

**65nm**

Package

**544 HSBGA**

Performance

**320 MFLOPS/1040 MIPS**

Power supply

**1,2V (core)/3,3V (I/O buffers)**

Power consumption

**Max 2,8W**

## Applications

- Professional high-precision programmable GNSS solutions
- Navigation programmable receivers
- Telecommunications
- Wide range of digital signal processing for SDR, general purpose computations and control functions

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# IP Cores

Module®
RESEARCH CENTRE

# IP CORES

Module has designed and tested RTL models of more than 40 IP cores. Some of them:

| No. | IP cores |
|---|---|
| 1 | Multichannel sound controller |
| 2 | CSA 3 descrambler |
| 3 | DVB-CI interface controller |
| 4 | NAND flash controller |
| 5 | Hardware 3DES accelerator |
| 6 | MPEG-2 Transport Stream Demultiplexer |
| 7 | HDTV video controller |

Tested and silicon-proven IP cores are available for order


РОССИЙСКАЯ ФЕДЕРАЦИЯ

СВИДЕТЕЛЬСТВО

о государственной регистрации программы для ЭВМ

№ 2010617803

Синтезируемая RTL-модель сложно-функционального блока аудиоконтроллера

Правообладатель(ли): *Закрытое акционерное общество Научно-технический центр «Модуль» (RU)*

Автор(ы): *Груздев Алексей Евгеньевич, Залётов Владимир Юрьевич, Севрюков Виктор Владимирович, Янкевич Евгений Александрович (RU)*

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*24 ноября 2010 г.*

*Руководитель Федеральной службы по интеллектуальной собственности, патентам и товарным знакам*

*Б.П. Симонов*

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# IP Core

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# CSA 3 DESCRAMBLER

## KEY FEATURES

- Full support of DVB CSA 3 Descrambling specification
- Flow-through architecture
- Up to 4 different transport streams
- APB 3.0 interface for programming
- About 100 K cells

## BENEFITS

- Easy to integrate with standard APB interface and simple flow-through data interface
- High performance – 5 cycle per byte
- Handling up to 4 different transport streams, even and odd keys for each

## APPLICATION

- DVB set-top-boxes with conditional access support and multiple tuners
- Personal video recorders
- Conditional Access Modules
- Broadcast equipment

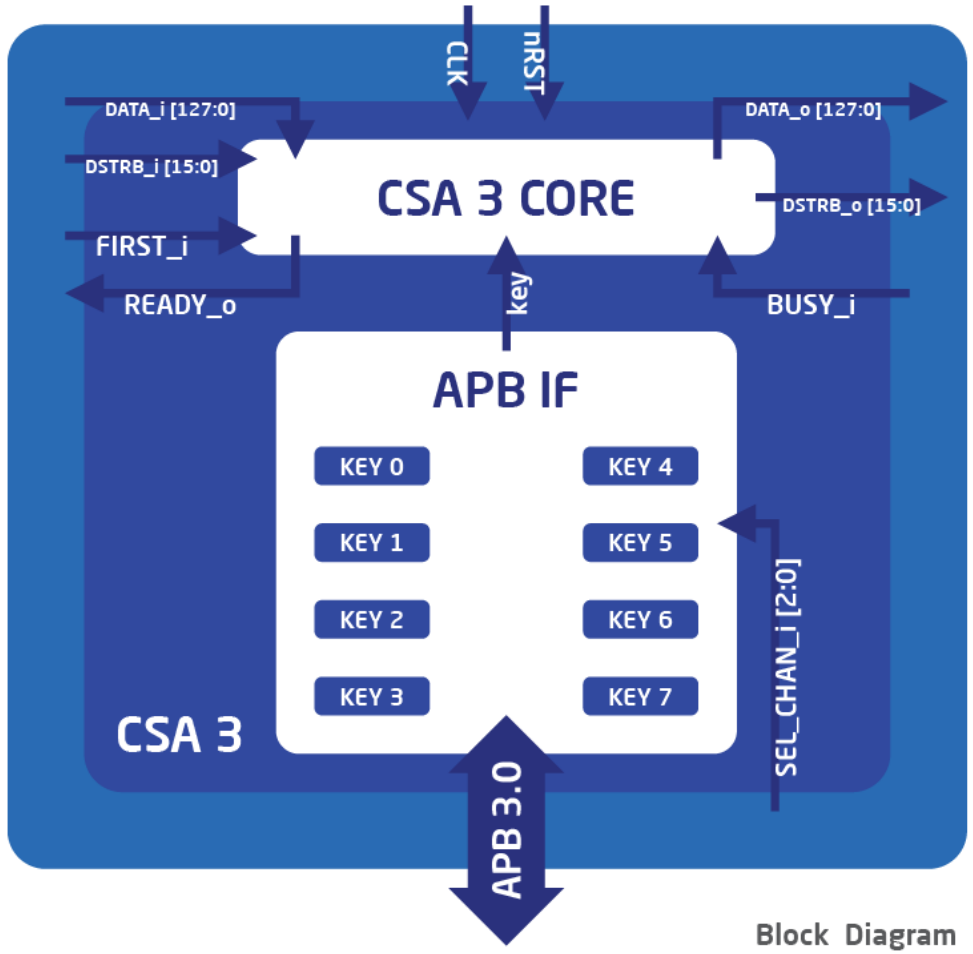
## RELATED IP

Transport Stream Demultiplexer
AES Crypto Core
DES Crypto Core
CSA 2.1 Descrambler

## OVERVIEW

The CSA 3 descrambler IP core is hardware implementation of DVB Common Scrambling Algorithm version 3. It was designed to remove protection from scrambled broadcast data by flow-through decryption of transport stream. It has simple custom interface for data with flow control and APB 3.0 slave interface (backward compatible with APB 2.0) for set keys.

The CSA 3 descrambler IP core was designed for handled up to four different transport streams with even and odd keys for each TS. Handling of one 128-bit data word takes about 78 clock cycles (i.e. about 5 clock cycles per 1 byte).




Block Diagram

# IP Core

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# NAND FLASH CONTROLLER

## KEY FEATURES

- Configurable Flash timing
- Supports ONFI 2.3 standard command set
- Only Asynchronous interface supported
- Up to 5 address cycles support
- Internal 2-Kbyte FIFO buffer
- 8-bit data bus
- Hardware ECC support 4, 24 bits correction
- Support interrupt driven functionality
- Hardware program/erase protection
- Supports both SLC and MLC chips
- Programmable block sizes
- Programmable page sizes from 0.5KB to 128KB
- AMBA APB Configuration Interface
- AMBA AXI 3.0 system interface
- DMA with big and little endian support
- Area 80000 Gates

## OVERVIEW

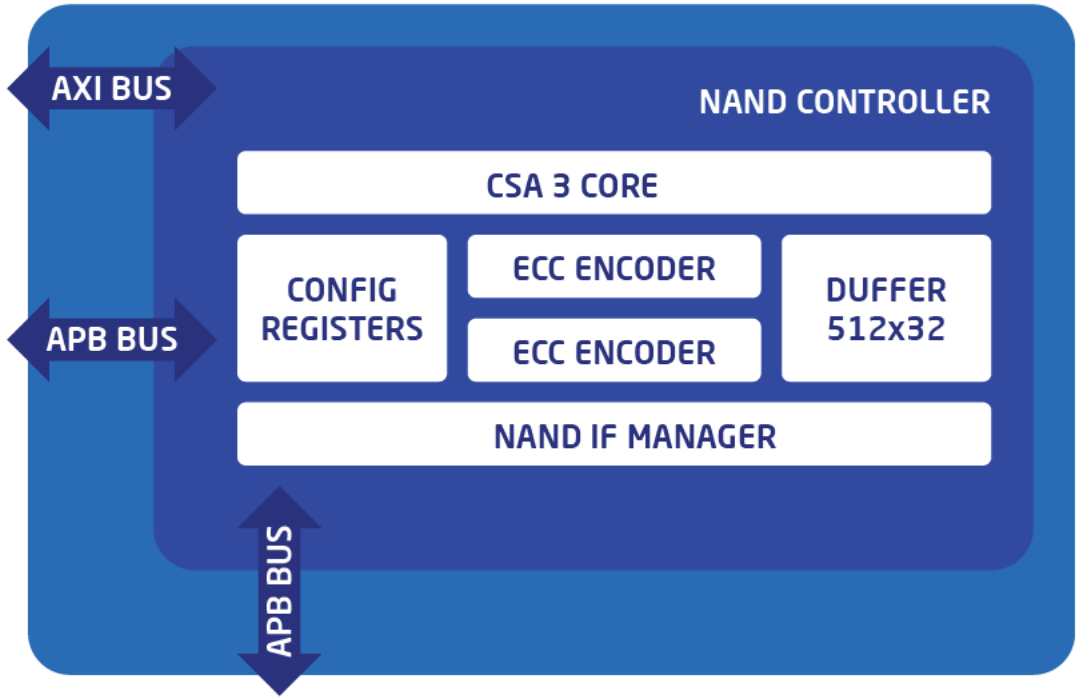
The NAND Flash controller IP core is used as a bridge between external NAND flash memory and master host system. It supports variety of memory manufacturers thanks to hardware ECC support up to 24 errors / 1KB and programmable page size, spare size and erase size. It is compliant to Open NAND Flash Interface (ONFI) 2.3 asynchronous mode supported. Built in DMA engine reduces CPU needs.

## APPLICATION

- DVB set-top-boxes
- USB Mass storage
- Network Storage
- Media Players
- Mobile Devices
- Portable Devices
- SSD

## BENEFIST

- Easy to integrate with standard configuration AMBA APB and AMBA AXI system interfaces
- Variety of supported flash chips




Block Diagram

# TSDEMUX

IP Core MPEG-2 Transport Stream Demultiplexer

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## KEY FEATURES

- ISO/IEC 13818-1 MPEG-2 complete support
- Simultaneous processing of 5 MPEG-2 transport streams: 3 external streams from tuners (serial/parallel), 2 stream from system memory
- Fast hardware PID filtering: 128 hardware PID filters, 32 independent DMA queues for writing filtered data to system memory
- Full and partial transport stream recording
- Pass-through mode
- Configurable parallel transport stream output interface
- AMBA 3 AXI Master and APB Slave system integration interfaces
- Descrambling on TS and PES levels: CSA2.1, CSA3.0, AES, DES/3DES
- 80 000 to 380 000 2-input NAND equivalent gates (depends on descramblers configuration), 24Kbit internal RAM

## BENEFITS

- Easy to integrate with standard AMBA interfaces
- Fast hardware PID filtering with 128 filters
- Up to 5 independent transport streams simultaneous processing
- High performance stream descramblers with multiple key sets and multiple algorithms support

## OVERVIEW

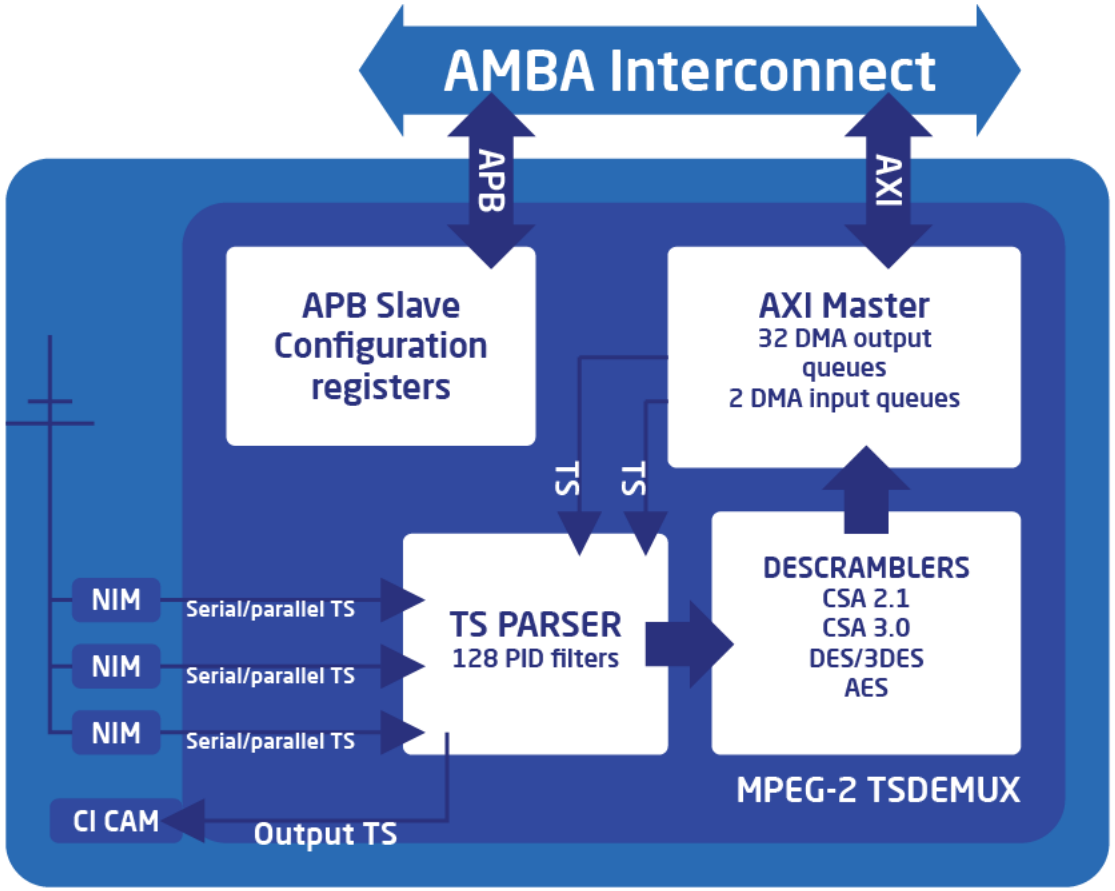
Transport Stream demultiplexer IP core (TSDEMUX) is a fully synthesizable IP block for MPEG-2 compatible digital TV equipment System-on-Chips. It can handle multiple Transport Streams from different tuners (over-the-air broadcasting) or system memory (IPTV, PVR). TSDEMUX can be configured to support up to 4 different descrambling algorithms for multiple Conditional Access Systems support. TSDEMUX IP minimizes host CPU usage in transport stream processing applications.

## APPLICATION

- DVB set-top-boxes with conditional access support and multiple tuners
- Personal video recorder
- Conditional Access Modules
- Broadcast equipment

## RELATED IP

- AES Crypto Core
- DES Crypto Core
- CSA 3 Descrambler
- CSA 2.1 Descrambler
- CRYPTO Accelerator




Block Diagram

NeuroMatrix® NMC3 DSP Core

Interval Timers IP Core

Synchronous Byte Communication I/O Port Controller

Vector Coprocessor IP Core

IP Core Multichannel Audio controller

Smart Card Interface Controller

NAND-Flash Controller IP Core

Transport Stream Demultiplexer IP Core

ARINC818 controller Transmitter and Reciever IP core

DVB CSA 3 Descrambler IP core

SpaceWire Channel Controller

Cryptograhpic DMA (RMACE) IP-core

NMU Processor System on the NMC3

Test Port Controller IP Core

External Memory Controller

IP Core HDTV Video Controller

Clock-Reset Generator (CRG)

DVB CI Controller

Crypto-accelerator Core

FiberChannel controller IP-core

DVB CSA 2.1 Descrambler IP core

DisplayPort Video Output Device

SPI Controller with DMA

3DES IP-core

SRAM/NOR Memory Controller with ECC IP Core

AES IP Core

Stream Crypto-accelerator IP Core

Video Capture Unit IP Core

I2S-RX IP-core

SDI-TX IP-core

Audio Output Device of the SPDIF standard

External Interrupt Controller

DMA Controller

Memory Protection Unit

SPDIF-RX IP-core

Video Display Unit IP-core

I2S-TX IP-core

Module® RESEARCH CENTRE

# TRAFFIC MONITOR®

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TrafficMonitor® is a family of software products designed for video surveillance of a road section, for real time measuring the traffic flow characteristics, and for transmitting the measured information to a remote traffic control station.

## TRAFFIC MONITOR PROVIDES THE FOLLOWING FUNCTIONAL TASKS:

### Simultaneous analysis of multiple lanes (6 lanes)

### The classification of vehicles

(cars; pick-ups and trucks up to 11 meters; trucks in length from 11 to 14 meters; trucks are longer than 14 meters; buses; motorcycles)

### Automatic detection of events on each band

(stop the vehicle; speed exceeding; opposite direction movement; start and end stage of traffic jams)

### Measurement of traffic characteristics for each lane separately

(total number of vehicles, passing in a fixed time; number of vehicles of each type; average speed for all vehicles; average speed of vehicles of each type; standard deflection of speed; average distance between vehicles; average interval time between vehicles; evaluation of lane congestion in percentage)

## THE SOFTWARE INCLUDES THE FOLLOWING:

### TMServer

Software network video detector

### TMKernel

Software video detector module

### TMControl

TMServer control application

### TMAPI

Application programming interface

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# Thank You!