COMPANY PROFILE

Founded: 1990  
Number of employees: 650

- Integrated Circuit Design (microelectronic design services),
- Design and manufacture of special computational modules, control systems for special applications (onboard and aviation equipment)
- Production and design of video recognition and analysis systems (DSP)
- Introduction of neural networks in modern automated complexes of various industries: from navigation and radar to unmanned vehicles and robotics
NEUROMATRIX® ARCHITECTURE

1995 - Module has started development of NeuroMatrix® architecture. The architecture is optimized for matrix multiplication algorithms and capable of dynamic precision and performance.

• A specific feature of this architecture is an authentic high-performance vector-matrix coprocessor
• The efficiency of the matrix multiplication operation is close to the theoretical peak
• Low power consumption allows the NeuroMatrix® processors to be used in embedded devices for emulation of deep convolutional networks
• 4 generations of NeuroMatrix® architecture implemented
• The latest generation (NMC4) featuring hardware support of floating-point computation

nmDL software package (Neuro Matrix for Deep Learning) has been developed to apply the trained deep neural networks on the NeuroMatrix® platform (TensorFlow® or Caffe® libraries).
Russian NeuroMatrix® processors

1995

- NM6403
- Class - 32/64-bit RISC / DSP fixed and floating point
- Highest performance on vector-matrix operations (neural networks, processing of radar, video and signal data)
- Dynamically changing performance to bit ratio
- Patents of the Russian Federation, USA and Korea

2019

- NM6408

Main applications

Radar, video processing, neural networks, robotics, GNSS, SDR navigation and communications, astro-orientation, digital television, multimedia, etc.
NM6406
High performance DSP processor

NM6406 is a high performance DSP processor designed for real time data flow processing. The architecture is based on the advanced VLIW/SIMD NMC3 core, and consists of a 32/64-bit RISC processor and a 64-bit VECTOR co-processor. The co-processor supports vector/matrix operations with elements of variable bit length (US Pat. 6539368 B1)

Features

Applications

• IR and video processing
• Navigation
• CDMA и TDMA base station

CMOS technology
Package
Clock frequency
90nm
416 BGA
320 MHz

Power supply

1.2 V (core) 3.3 V (I/O buffers)

Power consumption

less than 1.2 W

Performance

320 MIPS (960 MOPS)

Temperature range

-55°C ... +85°C.
1888BC048

A versatile 32-bit processor with a wide range of interfaces. Designed for use in embedded equipment.

Features

- CMOS technology
- Package: HSFCBGA-676
- Processor Architecture: ARM Cortex-A5

Power supply: 0.9V (core)/3.3V (I/O buffers)

Power consumption: 1.2 W

Temperature range: -60...+ 85 °C

Applications

- General and real-time information control system: as main SoC as interface south bridge
- Ethernet NIC with embedded hypervisor, etc
MM7705
HD Multimedia Processor

The chip is designed for use as a central processor for devices requiring high performance and high-energy efficiency in computing systems and devices for processing multimedia information.

<table>
<thead>
<tr>
<th>CMOS technology</th>
<th>Typical power</th>
<th>Maximum power</th>
<th>Processor Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>28 nm</td>
<td>8 W</td>
<td>15 W</td>
<td>PowerPC v2.05</td>
</tr>
</tbody>
</table>

Processors

2 CPUs (PowerPC 470S) and 4 DSPNMC3

Hardware video encoder / decoder

1080p high-definition, 60 frames per sec

DDR3 memory, 800-1600Mbps, 32 bits, 2 interfaces with the ability to connect up to 8 GB

Applications

- Onboard steering machines
- Input, output, processing, encoding / decoding multimedia information
- Switching and conversion of video streams
Neural Networks
NeuroMatrix neural network accelerators and computers

Embedded MC121.01 computer on the NM6407 processor

Neural network accelerator MC127.05 at NM6408 processor
**Neural Network Computer MC121.01**

MC121.01 is integrated circuit computer designed on the basis of a specialized neural microprocessor NM6407. The module is designed to function as part of a complex, in particular with a PC with USB 2.0 interface. This module is designed to perform a wide class of tasks related to digital signal processing in real time.

### Features

<table>
<thead>
<tr>
<th>Processor clock speed</th>
<th>Speed scalar operations</th>
<th>Speed vector operations</th>
<th>The total amount of memory</th>
<th>Power supply</th>
</tr>
</thead>
</table>
| 500 MHz               | Up to 500 million operations per sec | up to 12 billion operations per sec with byte operands | DDR2 SDRAM 512 MB | 2.5 W
|                       |                         |                         |                             | 5 to 12 V    |
NM6407
High performance neuro-processor for DSP operation

The neuro-processor NM6407MP is based on NeuroMatrix® architecture combining the features of two architectures of VLIW / SIMD processors. The chip contains two processor cores NMPU0 and NMPU1 with a RISC processor and a vector coprocessor for performing vector-matrix operations on integer data of variable length from 1 to 64 bits and floating point vector operations.

Features

<table>
<thead>
<tr>
<th>CMOS technology</th>
<th>Memory on a SoC</th>
<th>Synchronization frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>65nm</td>
<td>16 Mbit</td>
<td>500 MHz</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltagess</th>
<th>Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0V (core), 1.8V (DDR2), 3.3V</td>
<td>Typical 2.4 W Max 7 W</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Performance</th>
<th>Temperature range</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 GFLOPs</td>
<td>-45 °C ... + 85 °C</td>
</tr>
</tbody>
</table>
Neural Network Accelerator MC127.05

The **MC127.05** is a high performance computing module with interface capabilities designed to be used as a universal hardware and software platform to receive, process, store and transfer large data in real time. The module can be applied as part of integrated systems to build a wide range of DSP and computer vision systems. The device is based on a heterogeneous high performance NM6408 neuroprocessor, consisting of 16 NM4 cores and five ARM Cortex-A5, five DDR3 controllers and a PCI-E2.0 interface.

**Features**

- integrated circuit NM6408;
- 5 banks of DDR3 memory, with a total capacity of 5 GB,
- bandwidth up to 32 GB / s;
- PCIe2.0 x4 with a throughput of 4 GB / s;
- Ethernet 100 Mb/s (with EDCL support);
- High-speed communication ports with a capacity of up to 16 GB/s;
- microSD, GPIO (28 pins), JTAG;
- Power consumption - 15W;
- Power supply - 12V;
- PCIe x16 Form Factor, 2 Slots

**Applications**

- Neural networks and artificial intelligence
- Specialized high-performance complexes
- Digital Signal and Image Processing Systems
- Machine vision systems
- Robotics
Applications
- Deep Neural Networks
- SDR navigation and communication
- Video processing
- Radiolocation
- 3D computer vision
- Hybrid high-performance computing systems

NM6408
High performance neuro-processor

The universal neuro-microprocessor is designed for a wide range of tasks, especially in emulation of neural networks and deep learning for special purposes.

NM6408 is capable of performing complex of operations connected with processing big data streams in real time: digital signal processing (DSP), image processing (recognition), navigation, communication, etc.

Features
- CMOS technology: 28 nm
- Performance: 512 GFLOPs
- Power consumption: 20W
- Power supply: 0.9V (core)/1.8V (I/O buffers)
- Package: 1444 HFCBGA
NeuroMatrix Neural Network Ecosystem

**Learning**
- NeuroMatrix® NM6408
- Neural Net Accelerator MC127.05
- Supercomputer for neural networks training
- Deep Learning Framework

**Inference**
- NeuroMatrix® NM6407
- Embedded Computer MC 121.01
- Tool software (SDK)
  - NMDL
  - NeuroMatrix® Deep Learning
Neuro Network Platform Key Elements

NMDL (Neuromatrix® Deep Learning) a set of hardware and software for the development and implementation of deep neural networks on NeuroMatrix® processors
NeuroMatrix Neuro Network Platform

Neural network training
(Learning)

NeuroMatrix®
NM6408

5G

Neuro networks implementation
(Inference)

NeuroMatrix®
NM6407

Hardware and software systems:
- Telemedicine
- Smart transport
- Smart city
- Smart factories
- Drones
- Virtual reality
- Security systems
- Finance
Operational Amplifiers
OAs are used in schemes with deep negative feedback, which completely determines the gain / transmission coefficient of the resulting circuit. On the basis of OA it is possible to build many different electronic components.

OAVF1/OAVF2

OACF1 - one-channel high-speed operational amplifier with voltage feedback.
OACF2 - two-channel operational amplifier with voltage feedback.
Amplifiers provide high-dynamic accuracy in a wide frequency range and stable operating at gains up to $AC = +1$. The architecture of the input stages implemented on the bridge differential amplifier provides the **slew rate of the output signal and the cutoff frequency of the maximum power** previously achieved only in broadband amplifiers with current feedback.

**Features**

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Maximum output voltage</th>
<th>The slew rate of amplifier</th>
</tr>
</thead>
<tbody>
<tr>
<td>210 MHz ($AC = +2$)</td>
<td>7.2 V ($U = \pm 5$ V)</td>
<td>940 V / µs</td>
</tr>
</tbody>
</table>

Output current: 130 mA
Temperature range: 60 to +125 °C
20ACF

Two-channel operational amplifier (OA) with current feedback

It provides good dynamic parameters in a wide range of frequencies and gains, **stably operating on a low-impedance load with gains up to AC = +3 and RH = 10 ohms**. In the OS, the function of turning off each channel is implemented independently, which takes the outputs of the OA to a high-impedance state. The OA is intended for use in the transceiver path of a high-speed multiplexed data transmission channel (MCPD).

**Features**

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Maximum output voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>240 MHz (AC = +4)</td>
<td>7.6 V (U = ± 5 V)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>The slew rate of amplifier</th>
<th>Output current</th>
<th>Temperature range</th>
</tr>
</thead>
<tbody>
<tr>
<td>1030 V/µs</td>
<td>500 mA</td>
<td>60 to +125 °C</td>
</tr>
</tbody>
</table>

**Applications**

- Analog-to-digital converters
- Digital-to-analog converters
- Current-voltage converters
- Voltage-current converters
- AC/DC
Applications

- Voltage comparators
- Differential amplifiers and integrators
- Voltage and current stabilizers
- Analog calculators and signal generators
- Analog-to-digital converters
- Digital-to-analog converters
- Current-voltage, voltage-current converters

40ACF

Four-channel operational amplifier (OA) with current feedback

It is designed for use in the transceiver path of the high-speed multiplex data channel (MDC). Two op-amp channels are designed for large output currents (up to 500 mA) for the transmitter unit. The other two are smaller (up to 130 mA) and are used for the receiver unit. Transmitter channels operate on a low-impedance load with gains up to AC = +3 and RH = 10 Ohm and have the function of shutting down each channel, independently transforming the OA outputs into a high impedance state. The receiver channels operate at gains up to AC = +1.

Features

- Maximum output voltage: 7.6 V (UP = ± 5 V)
- The slew rate of amplifier: 1030 V / µs
- Frequency: 240 MHz (AC = +4)
- Output current: 500/130 mA
- Temperature range: 60 to +125 ° C
GNSS RECEIVER MC149.01

MC149.01 is a three-frequency receiver. It is designed to build high-precision consumer navigation equipment and provide centimeter-level accuracy in any kind of vehicles and automotive transport systems. Compatible with library of high precision navigation RTKLib for work with third-party navigation equipment manufacturers.

Centimeter accuracy (1σ) Location Accuracy (1σ)
in plan: 1 cm + 1 ppm offline mode: 2m
in height: 1.5 cm + 1 ppm SBAS: 0.75m

Applications
- GLONASS / GPS / GALILEO / COMPASS
- Cellular signal receivers
- Digital broadcasting (DAB)
- Autonomous cars
- Robotics and drones
- Agriculture (precision farming)
- Geodesy

Applications
- GLONASS L1OF, L2OF, L3OC, GPS L1 C / A, L2CM, L5

Hardware support
- BeiDou B1 / B2. Galileo E1 / E5a / E5b. QZSS L1 / L2
- 20Hz navigation solution temp

Voltage Power consumption
3.7 - 8.4 V 1.6 - 1.8 W3
BBP2
High performance DSP processor (navigation)

The chip is designed for creating high-performance measurement modules that provide reception and processing GNSS GLONASS / GPS / GALILEO signals and SBAS functional add-ons in navigation equipment. It provides information on the integrity of the navigation field, corrects the information about the exact coordinates of the satellites and the time-frequency parameters of the system.

Features

<table>
<thead>
<tr>
<th>Applications</th>
<th>Features</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Professional high-precision programmable GNSS solutions</td>
<td>CMOS technology 65nm</td>
<td>320 MFLOPS/1040 MIPS</td>
</tr>
<tr>
<td>Navigation programmable receivers</td>
<td>Package 544 HSBGA</td>
<td></td>
</tr>
<tr>
<td>Telecommunications</td>
<td>Power supply 1,2V (core)/3,3V (I/O buffers)</td>
<td>Power consumption Max 2,8W</td>
</tr>
<tr>
<td>Wide range of digital signal processing for SDR, general purpose computations and control functions</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
IP Cores
Module has designed and tested RTL models of more than 40 IP cores. Some of them:

<table>
<thead>
<tr>
<th>No.</th>
<th>IP cores</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Multichannel sound controller</td>
</tr>
<tr>
<td>2</td>
<td>CSA 3 descrambler</td>
</tr>
<tr>
<td>3</td>
<td>DVB-CI interface controller</td>
</tr>
<tr>
<td>4</td>
<td>NAND flash controller</td>
</tr>
<tr>
<td>5</td>
<td>Hardware 3DES accelerator</td>
</tr>
<tr>
<td>6</td>
<td>MPEG-2 Transport Stream Demultiplexer</td>
</tr>
<tr>
<td>7</td>
<td>HDTV video controller</td>
</tr>
</tbody>
</table>

Tested and silicon-proven IP cores are available for order.
IP Core

www.module.ru
sales@module.ru
+7 495 591 80 80

OVERVIEW
The CSA 3 descrambler IP core is a hardware implementation of DVB Common Scrambling Algorithm version 3. It was designed to remove protection from scrambled and broadcast data by flow-through decryption of transport stream. It has a simple custom interface for data with flow control and APB 3.0 slave interface (backward compatible with APB 2.0) for set keys.

The CSA 3 descrambler IP core was designed for handling up to four different transport streams with even and odd keys for each TS. Handling of one 128-bit data word takes about 78 clock cycles (i.e., about 5 clock cycles per 1 byte).

KEY FEATURES
• Full support of DVB CSA 3 Descrambling specification
• Flow-through architecture
• Up to 4 different transport streams
• APB 3.0 interface for programming
• About 100 K cells

BENEFITS
• Easy to integrate with standard APB interface and simple flow-through data interface
• High performance – 5 cycle per byte
• Handling up to 4 different transport streams, even and odd keys for each

APPLICATION
• DVB set-top-boxes with conditional access support and multiple tuners
• Personal video recorders
• Conditional Access Modules
• Broadcast equipment

RELATED IP
Transport Stream Demultiplexer
AES Crypto Core
DES Crypto Core
CSA 2.1 Descrambler
IP Core

OVERVIEW
The NAND Flash controller IP core is used as a bridge between external NAND flash memory and master host system. It supports variety of memory manufacturers thanks to hardware ECC support up to 24 errors / 1KB and programmable page size, spare size and erase size. It is compliant to Open NAND Flash Interface (ONFI) 2.3 asynchronous mode supported. Built-in DMA engine reduces CPU needs.

APPLICATION
- DVB set-top-boxes
- USB Mass storage
- Network Storage
- Media Players
- Mobile Devices
- Portable Devices
- SSD

BENEFITS
- Easy to integrate with standard configuration AMBA APB and AMBA AXI system interfaces
- Variety of supported flash chips

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Tel: +7 499 152 96 98. Fax: +7 499 152 46 61.
**KEY FEATURES**

- ISO/IEC 13818-1 MPEG-2 complete support
- Simultaneous processing of 5 MPEG-2 transport streams
- 3 external streams from transport stream
- Audio/Video PID filtering
- 1/288 hardware PID filters
- 3/2 independent DMA queues for writing filtered data to system memory
- Full and partial transport stream
- Full transport stream recording
- Pass-through mode
- Configurable parallel transport stream output
- AMBA 3 AXI Master and APB Slave system interfaces
- Descrambling on TS and PES levels: CS2.1, CSA/B, AES, DES/3DES
- 90 000 to 300 000 2-input NAND equivalent gates (depends on descramblers configuration), 256kB internal RAM

**BENEFITS**

- Easy to integrate with standard AMBA interfaces
- Fast hardware PID filtering with 1/288 filters
- Up to 5 independent transport stream simultaneous processing
- High-performance stream descramblers with multiple key sets and multiple algorithms support

**OVERVIEW**

Transport Stream demultiplexer IP core (TSDEMUX) is a fully synthesizable IP block for MPEG-2 compatible digital TV equipment System-on-Chips. It can handle multiple Transport Streams from different tuners (over-the-air broadcasting) or System memory (PTV, PVR). TSDEMUX can be configured to support up to 4 different descrambling algorithms for multiple Conditional Access Systems support. TSDEMUX IP minimizes host CPU usage in transport stream processing applications.

**APPLICATION**

- DVB set-top-boxes with conditional access support and multiple tuners
- Personal video recorder
- Conditional Access Modules
- Broadcast equipment

**RELATED IP**

- AES Crypto Core
- DES Crypto Core
- CSA 3 Descrambler
- CSA 2.1 Descrambler
- CRYPTO Accelerator

---

**Block Diagram**

- AMBA Interconnect
- APB Slave Configuration registers
- AXI Master 32 DMA output queues
- 2 DMA input queues
- DESCRAMBLERS: CSA 2.1, CSA 3.0, DES/3DES, AES

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Module®, and NeuroMate® are registered trade marks of RC Module, JSC. All other names are property of their respective owners. RC Module, JSC, Russia, Moscow, 125199, PVO 156, 3 Eight March 4th Street. Tel.: +7 495 152 96 98. Fax: +7 495 152 46 61
<table>
<thead>
<tr>
<th>NeuroMatrix® NMC3 DSP Core</th>
<th>NMU Processor System on the NMC3</th>
<th>SRAM/NOR Memory Controller with ECC IP Core</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interval Timers IP Core</td>
<td>Test Port Controller IP Core</td>
<td>AES IP Core</td>
</tr>
<tr>
<td>Synchronous Byte Communication I/O Port Controller</td>
<td>External Memory Controller</td>
<td></td>
</tr>
<tr>
<td>Vector Coprocessor IP Core</td>
<td>IP Core HDTV Video Controller</td>
<td></td>
</tr>
<tr>
<td>IP Core Multichannel Audio controller</td>
<td>Clock-Reset Generator (CRG)</td>
<td>Stream Crypto-accelerator IP Core</td>
</tr>
<tr>
<td>Smart Card Interface Controller</td>
<td>DVB CI Controller</td>
<td>Video Capture Unit IP Core</td>
</tr>
<tr>
<td>NAND-Flash Controller IP Core</td>
<td>Crypto-accelerator Core</td>
<td>I2S-RX IP-core</td>
</tr>
<tr>
<td>Transport Stream Demultiplexer IP Core</td>
<td>FiberChannel controller IP-core</td>
<td>SDI-TX IP-core</td>
</tr>
<tr>
<td>ARINC818 controller Transmitter and Receiver IP core</td>
<td>DVB CSA 2.1 Descrambler IP core</td>
<td>Audio Output Device of the SPDIF standard</td>
</tr>
<tr>
<td>DVB CSA 3 Descrambler IP core</td>
<td>DisplayPort Video Output Device</td>
<td>External Interrupt Controller</td>
</tr>
<tr>
<td>SpaceWire Channel Controller</td>
<td>SPI Controller with DMA</td>
<td>DMA Controller</td>
</tr>
<tr>
<td>Cryptographiipc DMA (RMACE) IP-core</td>
<td>3DES IP-core</td>
<td>Memory Protection Unit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SPDIF-RX IP-core</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Video Display Unit IP-core</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I2S-TX IP-core</td>
</tr>
</tbody>
</table>
TrafficMonitor® is a family of software products designed for video surveillance of a road section, for real-time measuring the traffic flow characteristics, and for transmitting the measured information to a remote traffic control station.

Traffic Monitor provides the following functional tasks:

- **Simultaneous analysis of multiple lanes (6 lanes)**
- **The classification of vehicles**
  - (cars; pick-ups and trucks up to 11 meters; trucks in length from 11 to 14 meters; trucks are longer than 14 meters; buses; motorcycles)
- **Automatic detection of events on each band**
  - (stop the vehicle; speed exceeding; opposite direction movement; start and end stage of traffic jams)

Measurement of traffic characteristics for each lane separately

- (total number of vehicles, passing in a fixed time; number of vehicles of each type; average speed for all vehicles; average speed of vehicles of each type; standard deflection of speed; average distance between vehicles; average interval time between vehicles; evaluation of lane congestion in percentage)

The software includes the following:

- **TMServer**
  - Software network video detector
- **TMKernel**
  - Software video detector module
- **TMControl**
  - TMServer control application
- **TMAPI**
  - Application programming interface